(12) PATENT APPLICATION PUBLICATION
(19) INDIA
(22) Date of filing of Application :05/03/2023

(21) Application No.202341014746 A
(43) Publication Date : 17/03/2023

(54) Title of the invention : VLSI layouts for connected and pyramid networks using deep neural learning

(51) International classification :G06F 303900, G06N 030400, G06N 030630, G06N 030800, G10L 253000
(86) International Application No :PCT//
Filing Date :01/01/1900
(87) International Publication No : NA
(61) Patent of Addition to Application Number :NA
Filing Date :NA
(62) Divisional to Application Number :NA
Filing Date :NA

(71)**Name of Applicant :**
**1)Midathada Vinay Kumar**
Address of Applicant :Assistant Professor, Department of Electronics and communication engineering, Avanthi Institute of Engineering and Technology Cherukupally village Beside Tagarapuvalasa Bridge Bhogapuram mandal Vizianagaram-531162 Vizianagaram ---------- ----------
**2)Dr.S Prema**
**3)Dr.P.Prakash**
**4)Anitha Mary M**
**5)Dr Sivaramakrishnan S**
**6)Dr. D. Raja Ramesh**
**Name of Applicant : NA**
**Address of Applicant : NA**
(72)**Name of Inventor :**
**1)Midathada Vinay Kumar**
Address of Applicant :Assistant Professor, Department of Electronics and communication engineering, Avanthi Institute of Engineering and Technology Cherukupally village Beside Tagarapuvalasa Bridge Bhogapuram mandal Vizianagaram-531162 Vizianagaram ---------- ----------
**2)Dr.S Prema**
Address of Applicant :Assistant Professor, Department of ECE, WWHG+28R, Golf Rd, Arivoli Nagar, Vivekanandapuram, Kovaipudur, Coimbatore,Tamil Nadu 641042 Coimbatore ---------- ----------
**3)Dr.P.Prakash**
Address of Applicant :Associate professor, Department of ECE, Sri Sairam Engineering college, Sai Leo Nagar,West tambaram, Tamil Nadu,Chennai-600044. Chennai ---------- ----------
**4)Anitha Mary M**
Address of Applicant :Assistant Professor(SS), Department of ECE, Rajalakshmi Engineering College, Thandalam, Chennai-602105. Tamil Nadu, India. Chennai ---------- ----------
**5)Dr Sivaramakrishnan S**
Address of Applicant :Associate Professor, Department of Information Science and Engineering, New horizon college of Engineering, Pincode 560103. Bangalore ---------- ----------
**6)Dr. D. Raja Ramesh**
Address of Applicant :Assistant Professor, Department of ECE, MVGR College of Engineering(A), Chintalavalasa, Vizianagaram-535005, Andhra Pradesh Vizianagaram ---------- ----------

(57) Abstract :
ABSTRACT VLSI LAYOUTS FOR CONNECTED AND PYRAMID NETWORKS USING DEEP NEURAL LEARNING Reducing the VLSI layout area of on-chip networks can result in lower costs and better performance. Those layouts that are more compact can result in shorter wires and therefore the signal propagation through the wires will take place in less time. The grid-pyramid network is a generalized pyramid network based on a general 2D Grid structure (such as mesh, torus, hypermesh or WK-recursive mesh). Such pyramid networks form a wide class of interconnection networks that possess rich topological properties. In this paper, we investigate these topologies from the VLSI-layout efficiency point of view. Also, we investigated on the layout of RTCC-pyramid networks that we believe can be considered in the class of Grid-pyramid networks.

No. of Pages : 21 No. of Claims : 7