A new topology of 31-level Multi level Inverter with Induction Motor

[1]Dhana Prasad Duggapu [2]Rajana Rajesh [3]Netinti Appanna [4]Vadisala Vinesh

[1]Assistant Professor, Dept. of EEE, Avanthi Institute of Engineering & Technology, Charukupally

[2,3,4] Student, Dept. of EEE, Avanthi Institute of Engineering & Technology, Charukupally

ABSTRACT

In this paper a new basic unit is proposed for multilevel inverters. The proposed basic units are used as building blocks to form a cascaded multilevel inverter i.e. the proposed topology consists of cascaded basic units and it uses lower number of switching devices and gate driver circuits. The design of proposed topology consists of mainly two parameters: the number of cascaded basic units and the number of dc sources in each basic unit. These two parameters can be used to design the desired multilevel inverter based on the operational conditions. Therefore the proposed topology offers good flexibility in designing. The comparison results with some recently introduced topologies showed that the proposed topology effectively reduces the components count. The simulation results obtained in MATLAB /SIMULINK as well as the experimental results of a 31-level inverter are presented and verified its performance.

Keywords: Total harmonic distortion, Multi-Level Inverter, Flying capacitor, Induction Motor and PWM Technique.

INTRODUCTION

Multilevel inverters have found their place in medium-voltage high-power applications such as electric motor drives, flexible ac transmission systems and static VAR compensators. The desired multi-staircase output voltage is obtained by combining several dc voltage sources. Solar cells, fuel cells, batteries and ultra-capacitors are the most common independent sources used. Multilevel inverters generate stepped output voltage by a proper arrangement of power electronic switches and several dc voltage sources. As the number of output voltage levels increases, the output voltage becomes more identical to a sinusoidal waveform resulting in lower distortions. Multilevel inverters have some advantages in comparison with the conventional two-level inverters including the use of low-voltage power electronic switches and improved output voltage quality. This results in the lower stress on the power electronic devices and lower losses.

Various circuit topologies are available for multilevel inverters. The conventional topologies are divided into three main types: the neutral point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB) multilevel inverters. The NPC multilevel inverters have the problem of balancing the voltage of capacitors for higher number of voltage levels. Also, they need considerable number of clamping diodes. Therefore this type of multilevel inverters is limited to three-level case. The FC multilevel inverter and it derivative topology stacked multi cell multilevel inverter use FCs to produce the voltage levels. These inverters have the ability of self-balancing of the capacitors so that they can be extended to higher number of output voltage levels easier than the NPC inverters. However, the FC inverters need high number of FCs for higher number of output voltage levels. The CHB multilevel inverters do not need clamping diodes and FCs. However, they need multiple isolated dc voltage sources. CHB multilevel inverters can be divided to symmetric and asymmetric topologies from the view point of values of the dc voltage sources. In the symmetric topologies, the values of all of the dc voltage sources are equal. These topologies have good modularity and share the voltage stress on the switches in the same way. However, they need very high number of components as the number of voltage levels increases. On the other hand, in all of the asymmetric topologies (including the proposed topology), the switches experience different stress. However, they use extremely lower number of components for a specific number of voltage levels. In this, a new cascaded asymmetric multilevel inverter is proposed. Firstly, a basic unit is proposed for the asymmetric multilevel inverter and then k basic units are cascaded to form the proposed asymmetric multilevel inverter. The proposed topology uses lower number of power electronic switches and gate driver circuits. In the next section the proposed topology and the algorithm for determining the values of dc voltage sources are described and then a comparison is presented. The simulation and experimental results of a 31-level inverter based on the proposed topology are presented to verify the capabilities of the topology.

I. PROPOSED TOPOLOGY OF 31-LEVEL INVERTER

The proposed multilevel inverter uses series connected basic units. The Proposed basic unit for the multilevel inverter is shown in Fig.2.1. The basic unit is a combination of two parts which are connected to each other by two switches SP and SN. Each part of the basic unit consists of n/2 dc voltage sources, two unidirectional switches and n/2 – 1 bidirectional switches. Such a two-part arrangement for the basic unit allows increasing the number of voltage levels since dc voltage sources with different values can be used in the two parts. It is important to mention that generally in the asymmetric condition the main aim is to maximize the number of voltage levels for a specific number of components. In all of the asymmetric topologies the modularity