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COMPARATIVE ANALYSIS OF PULSED LATCH AND FLIP-FLOP BASED SHIFT REGISTERS FOR HIGH-PERFORMANCE AND LOW-POWER SYSTEMS

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ABSTRACT
An optimized area-efficient shift register is proposed using pulsed latches. The area and power consumption are reduced by replacing flip-flops with pulsed latches. This method solves the timing problem between pulsed latches through the use of multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. A 64-bit shift register using pulsed latches was implemented by using an 180nm CMOS process with V_{DD} = 1.8V at the clock frequency of 100MHz.

KEYWORDS: *Flip-Flop, Pulsed Latch, CMOS Process, Non-Overlap*

I. INTRODUCTION

Low power circuit design has emerged as a principal theme in today's electronics industry. In the past, major concerns among researchers and designers for designing integrated circuits were on area, speed, and cost; while secondary importance was paid to power dissipation. In recent years, however, this scenario has changed and now developing of different circuit techniques for low power circuit design is an important research area. On designing any combinational or sequential circuits, the power consumption, implementation area, speed, voltage leakage, and efficiency of the circuit are the important parameters to be considered initially. These parameters are inter related to each other so in order to obtain few parameters remain may have less preference.

Shift register have several type of applications like data conversion between parallel to serial or serial to parallel, counters, parity generator, etc. Coming to the real time applications like image processing ICs [4]-[6], digital filters [1] and communication receivers [3] also we are using shift registers. Let consider the shift register application in image processing. As the size of the image data continues to increase due to the high demand for High quality image data, the word length of the shifter register increases to process large image data in image processing ICs [3]. As the word length of the shifter register increases, the area and power consumption of the shift register become important design considerations. Our proposed project is to reduce the power and area of the circuit by replacing the flip-flops with the latches in the shift register.

This paper is organized as follows. Section II provides an overview of the various types of Flip-Flops in terms of their advantages and drawbacks, and section III describes the analysis of proposed pulsed latch based shift register. Section IV provides schematics of Flip-Flop and Pulsed Latch based shift registers of various sizes and clock pulse generator which are drawn in S-Edit. Simulation results from HSPICE using 180nm PTM technology with V_{DD}=1.8V and their comparisons are presented in Section V and conclusion is drawn in Section VI.

II. CONVENTIONAL METHODS

In conventional method shift register is designed by serial connection of the master-slave flip flops. The following figure shows the master slave flip flop.