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LOW POWER FULL SWING XOR AND XNOR STRUCTURES FOR FULL ADDER CIRCUITS

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ABSTRACT

As the scale of integration increases, the usability of circuits is restricted by the more amounts of power and area consumption. The growing popularity demands for battery operated devices such as mobile phones, tablets and laptops. By reducing the number of transistors in the conventional circuits we have proposed two full adder circuits which is having advantage of consuming low power when compared to the other two conventional circuits. In this project XOR-XNOR gates are used to implement full adder structures. These circuits are going to be optimized in terms of power consumption and delay, which are due to low output capacitance adder. One-bit full adder circuit is proposed based on novel full-swing XOR-XNOR gates. To investigate the performance of the circuits Tanner Tools and HSPICE are used. This simulation is based on 90nm technology. The simulations result in high and speed and low power against other full adder designs. These circuits are to be simulated in the terms of variation of the supply, output capacitance and the size of transistors. These circuits have their own merits in terms of speed, power consumption, power delay product and driving ability

***INDEX TERMS*: Capacitance adder, Delay, Low power.**

I. INTRODUCTION

Today the electronic systems are a part of everyday life. Increased usage of operated portable devices, like cellular phones, personal digital assistants (PDAs) demand VLSI and ultra-scale large integration designs with an improved power delay Characteristics. The efficiency of many digital applications depends on performance of arithmetic circuits such as adders, multipliers, comparators and dividers. Full adders act as a core component of the complex circuits for multiplication and division and thereby influence the overall performance of the entire system. Full adder is a basic building block or component used in architectures of VLSI. Adder circuits are used in arithmetic logic circuit designs, processor chip like Snapdragon, Exynos, or Intel Pentium for CPU part.

In VLSI, the trade-off factors are low power consumption, delay, speed, cost. Several logic styles full adders [1]. Every circuit has its own advantages and disadvantages based on power and delay

The rest of the paper is organized as follows. In Section II the circuits for XOR-XNOR gates, Section III proposed circuits of XOR-XNOR gates and six new full adders are designed, Section IV consists of newly proposed Full adders Section V have the simulation results of the proposed circuits and Section V concludes the paper.

II. REVIEW OF XOR AND XNOR GATES

Figure 1 shows the Full Swing XOR/XNOR circuit designed by using Double pass – transistor logic (DPL) style [1]. This structure has 8 transistors. The main disadvantage of this circuit is using 2 NOT gates which consumes high power because NOT gates must drive output capacitance. Therefore, size of transistors in NOT gates should be increased to obtain lower delay with large capacitance it causes the creation of intermediate node. Therefore, power dissipation and short circuit power are increased, delay will also increase.

Figure 2 shows the Full Swing XOR/XNOR circuit designed by using Pass – transistor logic (PTL)[1] style. This structure has 6 transistors. This circuit has less delay and power consumption which are better than Figure 1. Here XOR circuit has lower delay than its XNOR circuit. The only problem in this circuit is using NOT gates in critical path. Delay is low in XNOR circuit because critical path of XOR circuit is composed of a NOT gate with NMOS transistor. But critical path of XNOR circuit is comprised of NOT gate and PMOS transistor which is slower than NMOS. Therefore, to