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AN OPTIMIZED LOW-VOLTAGE LOW-POWER DOUBLE TAIL COMPARATOR FOR HIGH-SPEED ANALOG TO DIGITAL CONVERTORS

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ABSTRACT

As today's world has become smart i.e,digitalization has been spreading rapidly, the need for ultra low-power ,area efficient and highspeed analog -to-digital converters is pushing towards the use of dynamic regenerative comparator to maximise the speed and power efficiency. In this paper, a dynamic double tail comparator with positive feed-back for latch regeneration has been designed with high-speed and low-offset. Simulations are carried out in 180nm and 90 nm CMOS technology. In the resultant comparator power dissipation and delay are reduced.

KEY WORDS: ***Digitalization, Dynamic, Double Tail, Latch Regeneration, Offset***

I. INTRODUCTION

In modern life, electronic equipment is frequently used in all fields such as communication, transportation, entertainment, medical, household etc. The requirement of analog to digital converters is increasing day by day as they play a major role in converting the analog signals to digital ones.ADCs act as interface between the natural analog world and the real time digital world. Comparator is the fundamental block which acts as heart of the ADC. In general ,a comparator is defined as an electronic device which compares the given analog input signal with reference voltage and produces a digital output i.e, either logic '0' or logic '1'. If the input to the non-inverting input is greater than that to the inverting input, the output is a logical 1. If the input to the non-inverting input is less than that to the inverting input, the output is a logical 0.

In this paper, Open loop comparators, pre-amplifier based comparators and dynamic comparators are discussed and a dynamic comparator is proposed to overcome the disadvantages of the previous topologies. The open loop comparator does not possess a clock input, due to which the output is generated randomly without a particular timing. On the other hand pre-amplifier based comparators make use of clock and achieve less offset voltage but suffer from static power dissipation and stacking [1]. This proposed dynamic comparator operated with low- voltage because of less stacking and achieves low-offset, high speed, low-power dissipation and high operating performance [1],[5].

This paper is organized as follows. Section II provides an overview of the various comparator topologies in terms of their advantages and drawbacks, and section III describes the analysis of proposed dynamic latched comparator. Section IV provides schematics of conventional and proposed dynamic latched comparators which are drawn in S-Edit. Simulation results obtained from HSPICE using 180nm and 90nm PTM technology [7] and their comparisons are presented in Section V and conclusion is drawn in Section VI.

II. COMPARATOR ARCHITECTURE AND TOPOLOGIES

Architectures of voltage comparators will be classified into three types: Open-loop Comparators (op-amps without compensation), Pre-amplifier