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DESIGN OF LOW-POWER HIGH-PERFORMANCE 2–4 AND 4–16 MIXED-LOGIC LINE DECODERS

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ABSTRACT

The invention of integrated circuits there has been a continuous demand for high performance, low power and low area or low cost diversified application from a variety of consumers. This demand has been pushing the fabrication process sub micron technologies such as 32, 22, 14nm and so on. The various technology aspects for low power applications are reviewed in detail, along with the evaluation of new technology, bearing in mind the power, performance and area. We are going to design 2-4 and 4-16 decoders with mixed logic design. Mixed logic is a gate-level design. It allows a digital logic circuit designer to separate the functional description of the circuit from its physical implementation. The use of mixed logic design provides logic expressions and logic diagrams that are analog of each other. In order to design these decoders there are two topologies are presented for the 2–4 decoder: a 14-transistor topology aiming on minimizing transistor count and power dissipation and 15-transistor topology aiming on high power-delay performance. Both normal and inverting decoders are implemented in each case, yielding a total of four new designs. Furthermore, four new 4–16 decoders will be designed by using mixed-logic 2–4 pre-decoders combined with standard CMOS post-decoder. All proposed decoders have full-swinging capability and reduced transistor count compared to their conventional CMOS counterparts. Finally, a variety of comparative spice simulations at some area by using these comparative simulations we can show that the proposed circuits present a significant improvement in power and delay, outperforming CMOS in almost all cases.

INDEX TERMS—*Line decoder, mixed-logic, power-delay optimization.*

I. INTRODUCTION

Very large scale integration (VLSI) is the process of creating an integrated circuit (IC) by combining thousands of transistors into a single chip. Over the past decade, power consumption of VLSI chips has constantly been increasing. Moore's Law drives VLSI technology to continuous increases in transistor densities and higher clock frequencies. The trends in VLSI technology scaling in the last few years show that the number of on-chip transistors increase about 40% every year. The operating frequency of VLSI systems increases about 30% every year. Although capacitances and supply voltages scale down meanwhile, power consumption of the VLSI chips is increasing continuously. On the other hand, cooling systems cannot improve as fast as the power consumption increases. Therefore in the very close future chips are expected to have limitations of cooling system and solving this problem will be expensive and inefficient.

The main objective of Analysis of low power high performance 2-4 and 4-16 mixed line logic decoders is to reduce the power consumption. The power consumption can be reduced by minimizing the transistor count by using mixed logic design when compared to CMOS logic design. We design 2-4 and 4-16 decoders using mixed logic as well as CMOS logic and compare the results between them. In VLSI systems there is a trade-off between three parameters those are power, area and speed. To obtain better results in two parameters the third parameter should be negligible. Here we are designing low power and high performance decoders