Course Structure
&
Detailed Syllabus

Department of
Electronics and Communication Engineering

M.Tech - VLSI Design

Academic Regulations - R24

Applicable for the Batches Admitted from 2024 - 2025

AVANTHI
INSTITUTE OF ENGINEERING AND TECHNOLOGY
(Autonomous)
(Approved by AICTE., New Delhi, & Permanently Affiliated to JNTU-GV, Vizianagaram)

NAAC "A+" Accredited Institute

Cherukupally (Village), Near Tagarapuvalasa Bridge, Vizianagaram (Dist)-531162

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

AVANTHI INSTITUTE OF ENGINEERING AND TECHNOLOGY

Vision and Mission of the Institute

Vision:

To develop highly skilled professionals with ethics and human values.

Mission:

1. To impart quality education with industrial exposure and professional training.
2. To produce competent and highly knowledgeable engineers with positive approach.
3. To develop self confidence among students which is an imperative pre-requisite to face the challenges of life.

Quality Policy:

Avanthi Institute of Engineering and Technology, Emphasizes the ethical ideals to impart advanced training by creating the best possible infrastructure engaging and activity oriented teaching. It also uses the most updated information an communication technology to promote a critical approach among the students and aims for an effective ambitious administration which is responsible in all the aspects.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

AVANTHI INSTITUTE OF ENGINEERING AND TECHNOLOGY

Programme: M.Tech -VLSI Design **Regulation: R24**

Vision and Mission of the Department

Vision:

To be a Centre of Excellence for High Quality Education and Research in the field of Engineering and Technology & human values with commitment of service for betterment of society and nation.

Mission:

M1: To facilitate young engineers to acquire technical exposure in the areas of Electronics and Communication Engineering.

M2: To prepare students for abrilliant career/entrepreneurship along with the development of knowledge, skills, attitude and team work for a successful professional career.

M3: To ensure effective teaching–learning process to provide in-depth knowledge of principles and its applications.

M4: To provide value based education by promoting the activities meeting the societal needs.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

AVANTHI INSTITUTE OF ENGINEERING AND TECHNOLOGY

Programme: M.Tech -VLSI Design **Regulation: R24**

Program Outcomes

PO1: Demonstrate knowledge with ability to select, learn and apply appropriate techniques, skills and modern engineering tools to solve engineering problems appropriate to the relevant discipline.

PO2: Analyze engineering problems critically, conceptualize, design, implement and evaluate potential solutions to contribute to the development of scientific/technological solutions in the context of relevant discipline.

PO3: Independently carry out research /investigation and development work to solve practical problems.

PO4: Function effectively as an individual and in a team to possess knowledge and recognize opportunities for career progression and research.

PO5: Communicate effectively in professional practice through verbal and written formats.

PO6: Recognize the need for self-motivated pursuit of knowledge to show commitment and competence in the broadest context of technological change.

Program Educational Objectives (PEOs)

PEO1: To educate and train the graduates with knowledge and skills necessary to formulate, design and solve problems in analog, digital & mixed signal VLSI Embedded system design, VLSI Signal processing & Hardware Software Co-design.

PEO2: Pursue career in research in the various fields of VLSI and Embedded Systems domain through self learning on cutting edge technologies

Program Specific Outcomes (PSOs)

PSO1: To design and develop VLSI circuits by learning advanced design techniques and algorithms to optimize design parameters requirement.

PSO2: Integration of embedded co-design for design methodologies in embedded & IoT applications.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Course Structure Program– M.Tech VLSI Design

(Applicable from the academic year 2024-2025 to 2026-2027)

I Year I Semester- Course Structure **Regulations: R24**

S.No	Category	Course Code	Course Title	Hours per Week			Credits
				L	T	P	
1	PC	MTVDPC1101	**Professional Core - I** CMOS Analog IC Design	3	0	0	3
2	PC	MTVDPC1102	**Professional Core - II** CMOS Digital IC design	3	0	0	3
3	PE	MTVDPE11011 MTVDPE11012 MTVDPE11013	**Professional Elective - I** 1. VLSI Technology 2. Digital Design with FPGA 3. MEMS Technology	3	0	0	3
4	PE	MTVDPE11021 MTVDPE11022 MTVDPE11023	**Professional Elective - II** 1. Device Modeling 2. Nano-electronics 3. Algorithms for VLSI Design	3	0	0	3
5	CC	MTMB1105	Research Methodology & IPR	2	0	0	2
6	PC	MTVDPC1103	**Laboratory-1** CMOS Analog IC Design Lab	0	0	4	2
7	PC	MTVDPC1104	**Laboratory-2** CMOS Digital IC Design Lab	0	0	4	2
8	AC	MTVDAC1101 MTVDAC1102	**Audit Course - I** 1.Value Education 2. Developing Soft Skills and Personality	2	0	0	0
			Total	**16**	**0**	**8**	**18**

Category	Courses	Credits
PC: Professional Core Course	4	10
PE: Professional Elective Course	2	6
CC: Compulsory Course	1	2
AC: Audit Course	1	0
Total	**8**	**18**

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Course Structure Program– M.Tech VLSI Design

(Applicable from the academic year 2024-2025 to 2026-2027)

I Year II Semester- Course Structure **Regulations: R24**

S.No	Category	Course Code	Course Title	Hours per Week			Credits
				L	T	P	
1	PC	MTVDPC1205	**Professional Core - III** Mixed Signal & RF IC Design	3	0	0	3
2	PC	MTVDPC1206	**Professional Core - IV** Physical Design Automation	3	0	0	3
3	PE	MTVDPE12031 MTVDPE12032 MTVDPE12033	**Professional Elective - III** 1. VLSI Signal Processing 2. IOT & its Applications 3. Physics of VLSI Devices	3	0	0	3
4	PE	MTVDPE12041 MTVDPE12042 MTVDPE12043	**Professional Elective - IV** 1. Embedded System Design 2. Microcontrollers & programmable Digital Signal Processors 3. Low Power VLSI Design	3	0	0	3
5	PR	MTVDPR1201	Mini project	2	0	0	2
6	PC	MTVDPC1207	**Laboratory-1** Mixed Signal IC Design Lab	0	0	4	2
7	PC	MTVDPC1208	**Laboratory-2** Physical Design Automation Lab	0	0	4	2
8	AC	MTVDAC1203 MTVDAC1204	**Audit Course - II** 1. English for Research Paper Writing 2. Constitution of India	2	0	0	0
			Total	**16**	**0**	**8**	**18**

Category	Courses	Credits
PC: Professional Core	4	10
PE: Professional Elective	2	6
PR: Project	1	2
AC: Audit Course	1	0
Total	**8**	**18**

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Program: M. Tech. VLSI Design Regulation: R24

II Year I Semester- Course Structure

S.No.	Category	Course Code	Course Title	Hours per Week			Credits
				Lecture	Tutorial	Practical	
1	PE	MTVDPE21051 MTVDPE21052 MTVDPE21053	**Professional Elective - V** Nano Materials and Nano Technology Digital System Design and Verification Photonics	3	0	0	3
2	OE		**Open Elective - I**	3	0	0	3
3	Dissertation	MTVDPJ2101	Dissertation Phase-I /Industrial Project (to be continued and evaluated next semester)	0	0	20	10
			Total	**6**	**0**	**20**	**16**

Category	Courses	Credits
PE: Professional Elective	1	3
OE: Open Elective	1	3
Dissertation	1	10
Total	**3**	**16**

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Program: M. Tech. VLSI Design Regulation: R24

II Year II Semester- Course Structure

S.No	Category	Course Code	Course Title	Hours per Week			Credits
				Lecture	Tutorial	Practical	
1	**Dissertation**	MTVDPJ2201	Project/ Dissertation Phase-II (continued from III semester)	0	0	32	16
			Total	**0**	**0**	**32**	**16**

Category	Courses	Credits
Dissertation	1	16
Total	**1**	**16**

OPEN ELECTIVES OFFERED BY DEPARTMENT OF ECE TO OTHER DEPARTMENT PG COURSES

OPEN ELECTIVE-I

COURSE CODE	COURSE NAME
MTVDOE2101	Fundamentals of Nano Technology
MTVDOE2102	Hardware Software Co-Design
MTVDOE2103	Digital CMOS VLSI Design
MTVDOE2104	Embedded Systems

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MTVDPC1101 **CMOS Analog IC Design** **3 0 0 3**

Course Objectives:

1. This course focuses on theory, analysis and design of analog integrated circuits in both Bipolar and Metal-Oxide-Silicon (MOS) technologies.
2. Basic design concepts, issues and trade-offs involved in analog IC design are explored.
3. Intuitive understanding and real-life applications are emphasized throughout the course.
4. To learn about Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power Supply Rejection Ratio of Two-Stage Op Amps, Cascade Op Amps, Measurement Techniques of OP Amp.
5. To know about Characterization of Comparator, Two-Stage, Open-Loop Comparators. Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators etc.

At the end of the course, students will be able to:

Course Code	Course Outcomes	Mapping with POs and PSOs								Dok
		PO1	PO2	PO3	PO4	PO5	PO6	PS01	PS02	
MTVDPC1101.1	Design MOSFET based analog integrated circuits.	3	2	3	1	0	1	3	0	L1,L2
MTVDPC1101.2	Analyze analog circuits at least to the first order.	3	2	3	1	0	1	3	0	L1,L2
MTVDPC1101.3	Appreciate the trade-offs involved in analog integrated circuit design	3	3	3	0	1	0	3	0	L3,L4
MTVDPC1101.4	Understand and appreciate the importance of noise and distortion in analog circuits.	2	3	3	1	0	1	3	2	L1,L4,L5
MTVDPC1101.5	Analyze and solve complex engineering problems critically in the domain of analog IC design for conducting research.	3	3	0	1	0	1	2	1	L2,L3,l5

SYLLABUS

UNIT –I **12 Hours**

Basic MOS Device Physics – General Considerations, MOS I/V Characteristics, Second Order effects, MOS Device models. Short Channel Effects and Device Models. Single Stage Amplifiers – Basic Concepts, Common Source Stage, Source Follower, Common Gate Stage, Cascode Stage.

COs–CO1

UNIT -II: **12 Hours**

Differential Amplifiers – Single Ended and Differential Operation, Basic Differential Pair, Common Mode Response, Differential Pair with MOS loads, Gilbert Cell. Passive and Active Current Mirrors– Basic Current Mirrors, Cascode Current Mirrors, Active Current Mirrors.

COs–CO2

UNIT -III: **12 Hours**

Frequency Response of Amplifiers – General Considerations, Common Source Stage, Source Followers, Common Gate Stage, Cascode Stage, Differential Pair. Noise – Types of Noise, Representation of Noise in circuits, Noise in single stage amplifiers, Noise in Differential Pairs.

COs–CO3

UNIT -IV: **12 Hours**

Feedback Amplifiers – General Considerations, Feedback Topologies, Effect of Loading. Operational Amplifiers – General Considerations, One Stage Op Amps, Two Stage Op Amps, Gain Boosting, Common – Mode Feedback, Input Range limitations, Slew Rate, Power Supply Rejection, Noise in Op Amps. Stability and Frequency Compensation. **COs–CO4**

UNIT -V: **12Hours**

Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

COs–CO5

Board of Studies : Electronics and Communication Engineering
Approved in BoS No: 01, 3rd August, 2024
Approved in ACM No: 01

Text Books:

1. B.Razavi, "Design of Analog CMOS Integrated Circuits", 2nd Edition, McGraw Hill Edition2016.
2. Paul. R.Gray& Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits", Wiley,5th Edition, 2009.

Reference Books:

1. T. C. Carusone, D. A. Johns & K. Martin, "Analog Integrated Circuit Design", 2nd Edition,Wiley, 2012.
2. P.E.Allen&D.R. Holberg, "CMOS Analog Circuit Design", 3rd Edition, Oxford University Press, 2011.
3. R. Jacob Baker, "CMOS Circuit Design, Layout, and Simulation", 3rd Edition, Wiley, 2010.

Web References:

1. https://onlinecourses.nptel.ac.in/noc20_ee26/preview
2. https://www.coursera.org/specializations/chip-based-vlsi-design-for-industrial-applications

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	30	20
L2	30	30
L3	40	40
L4	--	05
L5	--	05
Total (%)	**100**	**100**

Short and Long Answers Questions of Various Cognitive Levels:

L1: Remember

1. What is the typical shape of the I/V curve for a MOSFET in the saturation region?

2. What are short channel effects in MOSFETs, and why are they significant in modern semiconductor devices?
3. What is the key difference between single-ended and differential amplifier operation?
4. What is the typical frequency response characteristic of a common-source amplifier?
5. What is meant by "noise figure" in the context of electronic circuits

L2: Understand

1. Explain how short channel effects impact the threshold voltage and drain current of a MOSFET.
2. Explain how differential operation improves noise rejection compared to single-ended operation.
3. Explain how the cascode stage improves the frequency response and overall performance of an amplifier.
4. Describe how a differential pair amplifier's configuration affects its noise performance compared to a single-ended amplifier.
5. Describe the differences between series-shunt and series-series feedback topologies in terms of their effect on impedance and gain.

L3: Apply

1. Compare the I/V characteristics of a long-channel MOSFET to a short-channel MOSFET. What differences would you expect and why?
2. Given the frequency response data of an amplifier, determine its bandwidth and the point at which it starts to attenuate significantly.
3. Analyze how different design choices (e.g., resistor values, transistor biasing) affect the overall noise performance of a single-stage amplifier.
4. Given a feedback amplifier with a known open-loop gain and feedback factor, calculate the closed-loop gain of the amplifier.

L4: Analysing

1. Analyze the effect of increasing the drain resistance RDR_DRD on the voltage gain and output impedance of a common-source amplifier.
2. Analyze the impact of variations in transistor beta (β\betaβ) on the accuracy of the output current in a basic current mirror.
3. Analyze how the source bypass capacitor affects the low-frequency response of a common-source amplifier.
4. Analyze how the output impedance of a source follower affects its high-frequency response.

L5: Evaluating

1. Evaluate the performance of a single-ended amplifier versus a differential amplifier in terms of common-mode rejection ratio (CMRR) and linearity.
2. Evaluate the performance of a basic current mirror in terms of current matching and temperature stability. What are the limitations of this configuration?
3. Evaluate the trade-offs of using a source follower in terms of frequency response and impedance matching. What are the benefits and limitations?
4. Evaluate the trade-offs involved in using different types of feedback (e.g., voltage vs. current feedback) in terms of gain, bandwidth, and stability.

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MTVDPC1102 **CMOS Digital IC Design** **3 0 0 3**

Course Objectives:

1. To understand the fundamental properties of digital Integrated circuits using basic MOSFET Equations and to develop skills for various logic circuits using CMOS related design styles.
2. The course also involves analysis of performance metrics.
3. To teach fundamentals of CMOS Digital integrated circuit design such as importance of Pseudo logic, Combinational MOS logic circuits, and Sequential MOS logic circuits.
4. To teach the fundamentals of Dynamic logic circuits and basic semiconductor memories which are the basics for the design of high performance digital integrated circuits?

At the end of the course, students is able to:

Course Code	Course Outcomes	Mapping with POs and PSOs								Dok
		PO1	PO2	PO3	PO4	PO5	PO6	PS01	PS02	
MTVDPC1102.1	Demonstrate advanced knowledge in Static and dynamic characteristics of CMOS,	3	3	2	0	1	0	0	1	L1,L2
MTVDPC1102.2	Alternative CMOS Logics, Estimation of Delay and Power, Adders Design.	3	3	2	0	0	0	2	2	L1,L3
MTVDPC1102.3	Classify different semiconductor memories.	3	3	2	1	0	0	2	2	L3,L4
MTVDPC1102.4	Analyze, design and implement combinational and sequential MOS logic circuits.	3	3	2	1	1	0	1	2	L2, L5
MTVDPC1102.5	Analyze and solve complex engineering problems critically in the domain of digital IC design for conducting research.	3	3	2	1	0	1	2	3	L2,L6

SYLLABUS

UNIT-I: MOS Design **12 Hours**

Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic. **COs–CO1**

UNIT-II: Combinational MOS Logic Circuits: **12 Hours**

MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OAI gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates. **COs–CO2**

UNIT-III: Sequential MOS Logic Circuits **12 Hours**

Behaviour of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop. **COs–CO3**

UNIT-IV: Dynamic Logic Circuits **12 Hours**

Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits. **COs–CO4**

UNIT-V: Semiconductor Memories **12 Hours**

Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory- NOR flash and NAND flash. **COs–CO5**

Board of Studies : Electronics and Communication Engineering
Approved in BoS No: 01, 3rd August, 2024
Approved in ACM No: 01

Text Books:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici,TMH, 3rd Ed., 2011.

Reference Books:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan Borivoje Nikolic, 2nd Ed., PHI.

Web References:

1. https://onlinecourses.nptel.ac.in/noc21_ee09/preview
2. https://www.coursera.org/learn/vlsi-chip-design-and-simulation-with-electric-vlsi-eda-tool

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	30	20
L2	30	30
L3	40	40
L4	--	05
L5	--	05
Total (%)	**100**	**100**

Sample Short and Long Answers Questions of Various Cognitive Levels:

L1: Remember

1. What is a pseudo NMOS inverter, and how does it differ from a conventional CMOS inverter?
2. What are the basic configurations for CMOS NOR and NAND gates?
3. What do AOI and OAI gates stand for, and how are they implemented in CMOS logic?
4. What is an edge-triggered flip-flop, and how does it differ from level-triggered latches?

L2: Understand

1. Explain how a CMOS inverter operates when the input voltage is at logic high versus logic low.

2. Explain how a CMOS full adder performs binary addition. What role do the different transistors play in the full adder circuit?
3. Explain how a CMOS transmission gate operates as a switch. What are the key factors that affect its switching performance?
4. Describe the operation of an SR latch. How do the Set (S) and Reset (R) inputs affect the output states?
5. Explain the primary differences between DRAM, SRAM, and Flash memory in terms of structure, performance, and typical applications.

L3: Apply

1. Given the input conditions and transistor parameters, calculate the output voltages for a CMOS NOR gate and a CMOS NAND gate.
2. Given a Boolean expression, design an AOI or OAI gate to realize the expression. Provide the schematic diagram and explain the design.
3. Given a timing diagram for an edge-triggered flip-flop, determine the output state for various clock edges and input conditions.

L4: Analysing

1. Analyze how variations in the threshold voltage affect the noise margins and switching characteristics of a pseudo NMOS inverter.
2. Analyze how different input conditions affect the stability and state retention of a bistable element. What factors influence its ability to hold a state?
3. Analyze the timing behavior of a CMOS D latch. How do the setup and hold times affect its operation?
4. Analyze the trade-offs between DRAM and SRAM in terms of speed, density, power consumption, and cost. How do these factors affect their use in different computing scenarios?

L5: Evaluating

1. Evaluate the advantages and disadvantages of using a pseudo NMOS inverter compared to a CMOS inverter in terms of power consumption, speed, and area.
2. Evaluate the performance of CMOS AOI and OAI gates in a specific application. What factors influence the choice between AOI and OAI gates?
3. Evaluate the impact of flash memory types on system design. How do the choice of NOR versus NAND flash and their performance characteristics influence overall system design and performance?

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MTVDPE11011 **VLSI Technology** **3 0 0 3**

Course Objectives:

1. To Understand MOS Transistor Fundamentals, Analyze MOS Transistor Characteristics and Understand Threshold Voltage.
2. Learn Photolithography Techniques, Etching Processes.
3. Apply Knowledge to Fabrication Challenges.
4. Apply Design Rules to Layout Design.
5. Analyze Sequential Circuit Timing and understand Sequential System Design Methodologies.

At the end of the course, students will be able to:

Course Code	Course Outcomes	Mapping with POs and PSOs								Dok
		PO1	PO2	PO3	PO4	PO5	PO6	PS01	PS02	
MTVDPE11011.1	Understand the basics of MOS transistors and also the characteristics of MOS transistors.	3	2	3	1	0	1	2	2	L1,L2
MTVDPE11011.2	Learn about the MOS fabrication process and short channel effects.	3	3	3	1	1	0	2	2	L1,L3
MTVDPE11011.3	Learn about the basic rules in layout designing.	3	3	3	0	1	1	1	2	L3,L4
MTVDPE11011.4	Analyse various combinational logic networks and sequential systems.	3	2	2	1	1	0	2	3	L4,L5
MTVDPE11011.5	Develop skills in designing and analysing digital and analog circuits	3	2	3.	0	1	1	1	3	L1,L5

SYLLABUS

UNIT 1: MOS Transistors **12 Hours**

Introduction, The Structure of MOS Transistors, The Fluid Model, The MOS Capacitor, The MOS Transistor, Modes of Operation of MOS Transistors, Electrical Characteristics of MOS Transistors, Threshold Voltage, Transistor Trans conductance g_m, Figure of Merit, Body Effect, Channel-LengthModulation, MOS Transistors as a Switch, Transmission Gate. **COs–CO1**

UNIT 2: MOS Fabrication Technology **12 Hours**

Introduction, Basic Fabrication Processes, Wafer Fabrication, Oxidation, Mask Generation, Photolithography, Diffusion, Deposition. N-MOS Fabrication Steps, CMOS Fabrication Steps, n-Well Process, p-Well Process, Twin-Tub Process, Latch-Up Problem and Its Prevention, Use of Guard Rings, Use of Trenches, Short-Channel Effects-Channel Length Modulation Effect. Drain-Induced Barrier Lowering, Channel Punch Through, Hot carrier effect, Velocity Saturation Effect **COs–CO2**

UNIT 3: Layout Design Rules **12 Hours**

Scaling Theory, Scalable CMOS Design Rules, CMOS Process Enhancements, Transistors, Interconnects, Circuit Elements, Efficient layout Design techniques **COs–CO3**

UNIT 4: Combinational Logic Networks **12 Hours**

Layouts for logic networks. Delay through networks. Power optimization. Switch logic networks. Combinational logic testing **COs–CO4**

UNIT 5: Sequential Systems **12 Hours**

Memory cells and Arrays, clocking disciplines, sequential circuit Design, Performance Analysis, Power optimization, Design validation and testing. **COs–CO5**

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Text Books:

1. Principals of CMOS VLSI Design-N.H.EWeste, K. Eshraghian, 2nd Edition, Addison Wesley.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.
3. Low-Power VLSI Circuits and Systems,Ajit Pal, SPRINGER PUBLISHERS
   Modern VLSI Design – Wayne Wolf, 3rd Ed., 1997, Pearson Education.

Reference Books:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, AnanthaChandrakasan,
3. Borivoje Nikolic, 2nd Ed., PHI.

Web References:

1. https://swayam.gov.in/nc_details/NPTEL
2. https://www.coursera.org/specializations/chip-based-vlsi-design-for-industrial-applications

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	30	20
L2	30	30
L3	40	40
L4	--	05
L5	--	05
Total (%)	**100**	**100**

Sample Short and Long Answers Questions of Various Cognitive Levels:

L1: Remember

1. What is the role of the gate, drain, and source in a MOS transistor?
2. What are the key steps involved in the basic fabrication processes of semiconductor devices?
3. What is the purpose of photolithography in semiconductor fabrication?
4. Define "scalable CMOS design rules."
5. What is the role of design validation and testing in the circuit design process?

L2: Understand

1. Describe the concept of the "body effect" in MOS transistors.

2. Explain the process of wafer fabrication and its significance in semiconductor manufacturing.
3. Describe how the channel length modulation effect impacts the drain current in a MOS transistor.
4. How does sequential circuit design differ from combinational circuit design?
5. Define "clocking discipline" in the context of sequential circuits.

L3: Apply

1. Given a MOS transistor circuit, how would you determine the operating mode (cutoff, triode, or saturation)?
2. Given a set of CMOS design rules, apply them to design a basic digital circuit layout ensuring it adheres to the scalability requirements.
3. Apply power optimization techniques to a given digital circuit design and explain the expected benefits.
4. Apply power optimization techniques to a given circuit design and describe the expected benefits.

L4: Analysing

1. Compare the advantages and disadvantages of the twin-tub process versus the n-well and p-well processes.
2. Compare the behavior of a MOS transistor with a long channel versus a short channel with respect to channel length modulation.
3. Analyze the impact of scaling on transistor performance, including effects on power consumption, speed, and leakage current.
4. Analyze the trade-offs between different memory cell types in terms of area, speed, and power consumption.

L5: Evaluating

1. Evaluate the trade-offs between reducing channel length to increase transistor speed and the resultant increase in channel length modulation effects.
2. Evaluate the effectiveness of a proposed layout design technique for reducing interconnect resistance and capacitance in a densely packed CMOS circuit.
3. Evaluate different approaches to minimizing delay in logic networks and recommend the most effective strategy based on specific design constraints.
4. Assess the impact of clocking disciplines on the reliability and performance of a sequential circuit design.

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Avanthi Inst of Engg. & Tech. (Autonomous)
Cherukupally (V), Near Tagarapuvalasa Bridge,
Bhogapuram (M), Vizianagaram (Dist) 531162

MTVDPE11012 **Digital Design with FPGA** **3 0 0 3**

Course Objectives:

1. Understand the various abstraction levels in Verilog HDL and thus model tasks & functions at behavioural level.
2. Model the state machines using D and JK Flip Flops and design the complex combinational and sequential logic circuits using various constructs in Verilog.
3. Understand the types programmable logic devices and building blocks of FPGA and thus implement the design using Xilinx and ALTERA FPGAs.

At the end of the course, students will be able to:

Course Code	Course Outcomes	Mapping with POs and PSOs								Dok
		PO1	PO2	PO3	PO4	PO5	PO6	PS01	PS02	
MTVDPE11012.1	Understand various abstraction levels in Verilog HDL.	3	3	2	0	0	1	1	1	L1,L2
MTVDPE11012.2	design finite state machine using D and JK Flip Flop	3	3	3	1	1	1	2	1	L3,L4
MTVDPE11012.3	model sequential circuit using behavioural modelling.	3	3	2	1	0	0	2	1	L3,L4
MTVDPE11012.4	Design the complex combinational and sequential logic circuits using various constructs in Verilog.	3	3	2	0	1	1	1	1	L4,L5
MTVDPE11012.5	Understand programmable logic devices and various blocks exist in FPGA. Use EDA tool to design complex combinational and sequential circuits.	3	3	2	1	0	1	2	1	L2,L4,L5

SYLLABUS

UNIT 1: Verilog HDL – Data Flow & Structural Modeling **12 Hours**

Lexical Conventions - Ports and Modules – Operators - Gate Level Modelling - Data Flow Modeling - System Tasks & Compiler Directives - Test Bench. **COs–CO1**

UNIT 2: State Machine Design **12 Hours**

Definition of state machines -State machine as a sequential controller- Analysis of state machines using D and JK flip-flops - Design of state machines- State table and State assignment - Transition/excitation table - excitation maps and equations - logic realization- Design examples: Sequence detector, Serial adder, Vending machine. **COs–CO2**

UNIT 3: Verilog HDL – Behavioral Modeling **12 Hours**

Behavioral level Modeling- Procedural Assignment Statements- Blocking and Non-Blocking Assignments -Tasks & Functions - Useful Modeling Techniques. **COs–CO3**

UNIT 4: Verilog Modeling of Combinational Circuits and Sequential Circuits **12 Hours**

Behavioral, Data Flow and Structural Realization of Adders and Multipliers Synchronous and Asynchronous FIFO – Single port and Dual port ROM and RAM - FSM Verilog modelling of Sequence detector - Serial adder **COs–CO4**

UNIT 5: FPGA Architecture and Xilinx and ALTERA FPGAs **12 Hours**

Types of Programmable Logic Devices: PLA, PAL, CPLD - FPGA Architecture - Programming Technologies-Chip I/O- Programmable Logic Blocks- Fabric and Architecture of FPGA Xilinx Virtex 5.0 Architecture - Xilinx Virtex VI Architecture – ALTERA Cyclone II Architecture - ALTERA Stratix IV Architecture. **COs–CO5**

Board of Studies : Electrical and Electronics Engineering
Approved in BoS No: 01,3rd August, 2024
Approved in ACM No: 01

Text Books:

1. Ming-Bo Lin, Digital Systems Design and Practice: Using Verilog HDL and FPGAs, Create Space Independent Publishing Platform, Second Edition, 2015.
2. Michael D Ciletti, Advanced Digital Design with the Verilog HDL, Prentice Hall, Second Edition, 2011.

Reference Books:

1. Wayne Wolf, FPGA Based System Design, Prentices Hall Modern Semiconductor Design Series, 2011.
2. Charles H Roth Jr, Lizy Kurian John and Byeong Kil Lee Digital Systems Design using Verilog, Cengage Learning, First Edition, 2016.

Web References:

1. https://www.coursera.org/learn/intro-fpga-design-embedded-systems
2. https://onlinecourses.nptel.ac.in/noc24_cs61/preview

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	30	20
L2	30	30
L3	40	40
L4	--	05
L5	--	05
Total (%)	**100**	**100**

Sample Short and Long Answers Questions of Various Cognitive Levels:

L1: Remember

1. List the different types of operators available in Verilog or VHDL.
2. Define the role of a state machine as a sequential controller.
3. What is the difference between blocking and non-blocking assignments?
4. What is an FSM (Finite State Machine) in Verilog?
5. What are the key programming technologies used for programmable logic devices?

L2: Understand

1. Explain the importance of lexical conventions in HDL programming.
2. How does a state table help in designing a state machine?

3. Describe how procedural assignment statements are used in HDL to specify the behavior of a design.
4. How does a serial adder operate compared to a parallel adder?
5. Describe how FPGA architecture supports flexibility in digital circuit design.

L3: Apply

1. Develop a gate level model for a simple digital circuit and explain the modeling process.
2. Apply blocking and non-blocking assignments to create a specific behavioral model and explain the outcome
3. Implement a behavioral model for a 4-bit adder in HDL and explain the approach used.
4. Implement a simple digital circuit using FPGA architecture, detailing the steps for configuring the FPGA.

L4: Analysing

1. Analyze a given test bench to determine its effectiveness in verifying the functionality of an HDL module.
2. Analyze a state machine design to identify and correct any issues in the state table or state assignment.
3. Analyze the differences in performance and complexity between behavioral, data flow, and structural models of adders and multipliers.
4. Examine the programming technologies used for FPGA and analyze their impact on configuration speed and reliability.

L5: Evaluating

1. Evaluate the use of system tasks and compiler directives in improving the HDL code's debugging and simulation capabilities.
2. Evaluate the design of a state machine for a sequence detector, considering factors such as state table completeness and logic minimization.
3. Evaluate the effectiveness of different HDL modeling approaches (behavioral, data flow, structural) for implementing adders and multipliers based on specific design requirements.
4. Evaluate the suitability of Xilinx Virtex VI architecture for a high-performance digital signal processing application.

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MTVDPE11013 **MEMS Technology (Elective-1)** **3 0 0 3**

Course Objectives:

1. Understanding MEMS Fundamentals.
2. Learn about the different materials used in MEMS fabrication, such as silicon, polymers, and ceramics.
3. Study various fabrication techniques including photolithography, etching, and deposition processes.
4. Understand the mechanical, electrical, and thermal behaviours of MEMS devices.
5. Learn about the integration of MEMS devices with electronic systems and their packaging requirements.

At the end of the course, students will be able to:

Course Code	Course Outcomes	Mapping with POs and PSOs								Dok
		PO1	PO2	PO3	PO4	PO5	PO6	PS01	PS02	
MTVDPE11013.1	To understand the basic concepts of MEMS technology and working of MEMS devices.	3	3	2	1	0	1	2	0	L1,L2
MTVDPE11013.2	To understand and selecting different materials for current MEMS devices and competing Technologies for future applications	3	3	2	1	0	1	2	1	L1,L2
MTVDPE11013.3	To understanding the concepts of fabrication process of MEMS, Design and Packaging Methodology.	3	3	2	0	0	1	2	1	L2,L3
MTVDPE11013.4	To analyze the various fabrication techniques in the manufacturing of MEMS Devices	3	3	2	0	0	1	1	2	L3,L4.L5
MTVDPE11013.5	To analyze the Characteristics of various MEMS Devices	3	3	2	0	0	1	1	2	L3,L4.L5

SYLLABUS

UNIT-I: Introduction to MEMS **12 Hours**

Introduction to MEMS & Real world Sensor/Actuator examples (DMD, Air-bag, pressure sensors). MEMS Sensors in Internet of Things (IoT), Bio-Medical Applications **COs–CO1**

UNIT-II: MEMS Materials and Their Properties **12 Hours**

Materials (eg. Si, SiO2, SiN, Cr, Au, Ti, SU8, PMMA, Pt); Important properties: Young modulus, Poisson"s ratio, density, piezo-resistive coefficients, TCR, Thermal Conductivity, Material Structure.Understanding Selection of materials based on applications **COs–CO2**

UNIT-III: MEMS Fab Processes – 1 **12 Hours**

Understanding MEMS Processes & Process parameters for: Cleaning, Growth &Deposition, Ion Implantation & Diffusion, Annealing, Lithography. Understanding selection of Fab processes based on Applications. **COs–CO3**

UNIT-IV: MEMS Fab Processes – 2 **12 Hours**

Understanding MEMS Processes & Process parameters for: Wet & Dry etching, Bulk& Surface Micro machining, Die, Wire & Wafer Bonding, Dicing, Packaging. Understanding selection of Fab processes based on Applications. **COs–CO4**

UNIT-V: MEMS Devices **12 Hours**

Architecture, working and basic quantitative behaviour of Cantilevers, Micro heaters, Accelerometers, Pressure Sensors, Micro mirrors in DMD, Inkjet printer-head. Understanding steps involved in Fabricating above devices **COs–CO5**

Board of Studies : Electronics and Communication Engineering
Approved in BOS No: 01, 3rd August, 2024
Approved in ACM No: 01

Text Books:

1. An Introduction to Micro electromechanical Systems Engineering; 2nd Ed - by N.Maluf, K Williams; Publisher: Artech House Inc
2. Practical MEMS - by Ville Kaajakari; Publisher: Small Gear Publishing
3. Micro system Design - by S. Senturia; Publisher: Springer

Reference Books:

1. Analysis and Design Principles of MEMS Devices - MinhangBao; Publisher:Elsevier Science.
2. Fundamentals of Micro fabrication - by M. Madou; Publisher: CRC Press; 2 edition
3. Micro Electro Mechanical System Design - by J. Allen; Publisher: CRC Press
4. Micro machined Transducers Sourcebook - by G. Kovacs; Publisher: McGraw-Hill

Web References:

1. https://nptel.ac.in/courses/117105082
2. https://nptel.ac.in/courses/108106165
3. https://archive.nptel.ac.in/courses/108/108/108108113/
4. https://learning.edx.org/course/course-v1:EPFLx+memsX+3T2018/home

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	30	20
L2	30	30
L3	30	40
L4	05	--
L5	05	--
Total (%)	**100**	**100**

Sample Short and Long Answers Questions of Various Cognitive Levels:

L1: Remember

1. What does MEMS stand for, and what are its primary components?

2. List three real-world examples of MEMS sensors and actuators.
3. Define the following terms: ion implantation, annealing, and lithography.
4. Define bulk micromachining and surface micromachining.
5. What is the basic structure of a MEMS cantilever?

L2: Understand

1. Explain how a Digital Micromirror Device (DMD) works and its application in display technology.
2. Describe the role of pressure sensors in automotive airbag systems.
3. Explain the importance of Young's modulus in selecting materials for MEMS devices. How does it affect the performance of a MEMS structure?
4. Explain the basic operation of a micro heater. How does it generate heat and what are its typical applications?
5. Explain how a cantilever-based MEMS sensor works. What physical principles are involved in its operation?

L3: Apply

1. Given a scenario where you need to monitor temperature and humidity in a smart home, which MEMS sensors would you choose and why?
2. How would you implement MEMS pressure sensors in a wearable health monitoring device?
3. Given a MEMS device that requires high precision in creating small cavities, which etching process (wet or dry) would be more suitable, and why?
4. Select an appropriate bonding technique for a MEMS device that needs to be integrated with a silicon-based IC. Justify your choice based on the requirements of the integration.
5. Design a basic micro mirror system for a consumer electronic application. What specifications and materials would you choose?

L4: Analysing

1. Compare the advantages and disadvantages of MEMS sensors versus traditional sensors in terms of size, cost, and performance.
2. Analyze the impact of MEMS technology on the development of IoT devices. How does it improve their functionality and efficiency?
3. Analyze the trade-offs between using Cr and Au as metal layers in a MEMS device. Consider factors such as deposition methods, cost, and mechanical properties.
4. Analyze the impact of different deposition techniques (e.g., sputtering vs. chemical vapor deposition) on the performance of MEMS sensors. How do these techniques affect material properties and device functionality?
5. Discuss the challenges in fabricating micro mirrors for DMD systems and how these challenges are addressed in the manufacturing process.

L5: Evaluating

1. Evaluate the effectiveness of MEMS-based accelerometers in automotive airbag systems compared to older sensor technologies. What are the key factors influencing their performance?
2. Assess the potential benefits and limitations of integrating MEMS sensors in biomedical applications such as glucose monitoring or wearable ECG monitors.

3. Evaluate the choice of packaging methods for a MEMS pressure sensor. What factors would influence your decision, and which method would be most suitable for protecting the sensor while ensuring performance?
4. Assess the impact of different bonding techniques (die bonding vs. wire bonding) on the reliability and cost of MEMS devices. Which method would be preferable for a high-volume production scenario, and why?
5. Assess the impact of different inkjet printer-head designs on print quality and reliability. Which design offers the best balance between performance and ease of fabrication?

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MTVDPE11021 **DEVICE MODELLING** **3 0 0 3**

Course Objectives:

1. To learn the operation and its characteristics of bipolar devices.
2. To understand about the modeling of MOS Capacitor.
3. To learn the physics of 4-terminal MOSFET.
4. Understanding various effects of threshold tailoring implant on 4-terminal MOSFET.
5. To understand SOI MOSFET electrical characteristics.

At the end of the course, students will be able to:

Course Code	Course Outcomes	Mapping with POs and PSOs								Dok
		PO1	PO2	PO3	PO4	PO5	PO6	PS01	PS02	
MTVDPE11021.1	To understand the physics of 2-terminal MOS operation and its characteristics	2	3	2	2	1	1	2	1	L1,L2
MTVDPE11021.2	To understand the operation and characteristics of MOS capacitor	3	2	2	1	1	3	1	1	L1,L2
MTVDPE11021.3	To understand the physics of 4-terminal MOSFET operation and its characteristics	1	2	1	1	1	1	2	1	L3,L4
MTVDPE11021.4	To analyse the various effects of threshold tailoring implant on 4-terminal MOSFET	2	3	1	1	1	2	3	1	L4,L5
MTVDPE11021.4	To analyse the SOI MOSFET electrical characteristics	1	2	1	1	1	1	2	1	L4,L5

SYLLABUS

UNIT I **12 Hours**

2-terminal MOS device: threshold voltage modelling (ideal case as well as considering the effects of Qf, Φms and Dit.). **COs–CO1**

UNIT II **12 Hours**

C-V characteristics (ideal case as well as taking into account the effects of Qf, Φms and Dit);MOS capacitor as a diagnostic tool (measurement of non-uniform doping profile, estimation of Qf, Φms and Dit) **COs–CO2**

UNIT III **12Hours**

4-terminal MOSFET: threshold voltage (considering the substrate bias); above threshold I-V modelling (SPICE level 1,2,3 and 4). **COs–CO3**

UNIT IV **12Hours**

Sub threshold current model; scaling; effect of threshold tailoring implant (analytical modelling of threshold voltage using box approximation); buried channel MOSFET. Short channel, DIBL and narrow width effects; small signal analysis of MOSFETs (Meyer"smodel) **COs–CO4**

UNIT V **12Hours**

SOI MOSFET: basic structure; threshold voltage modelling Advanced topics: hot carriers in channel; EEPROMs; CCDs; high-K gate dielectrics. **COs – CO5**

Board of Studies : Electrical and Electronics Engineering
Approved in BOS No: 01, 3rd August, 2024
Approved in ACM No: 01

Text Books:

1. D.G.Ong , "Modern MOS Technology: Processes, Devices and Design", McGraw Hill,1984.
2. Y.Taur and T.H.Ning, "Fundamentals of modern VLSI Devices" Cambridge Univ. Press,1998.
3. S.M.Sze, "Physics of Semiconductor Devices" Wiley,1981.

Web References:

1. https://nptel.ac.in/courses/117/106/117106033/

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	30	20
L2	30	30
L3	40	40
L4	--	05
L5	--	05
Total (%)	**100**	**100**

Sample Short and Long Answers Questions of Various Cognitive Levels:

L1: Remember

1. What is device modeling, and why is it essential in semiconductor device design and development?
2. What are the different levels of device modeling (physical, compact, behavioral), and when is each appropriate to use?
3. Explain the concept of model order reduction and its importance in efficient device simulation.
4. Discuss the trade-offs between accuracy and computational efficiency in device modeling.
5. How do statistical process variations impact device modeling and circuit design?

L2: Understand

1. Explain the physical principles behind the drift-diffusion model for MOSFETs.
2. What are the limitations of the drift-diffusion model, and when does it break down?
3. Describe the concept of velocity saturation and its impact on MOSFET modeling.
4. How is short-channel effects modeled in MOSFETs, and what are the challenges involved?
5. Discuss the role of quantum effects in MOSFET modeling for advanced technology nodes

L3: Apply

1. How do you model bipolar junction transistors (BJTs) compared to MOSFETs?
2. What are the specific challenges in modeling devices like diodes, resistors, and capacitors?

3. How do you model interconnects and their impact on circuit performance?
4. Discuss the modeling of emerging memory devices (e.g., SRAM, DRAM, Flash memory).

L4: Analysing

1. What are the popular commercial and open-source device modeling tools available?
2. Compare and contrast different device modeling techniques (e.g., analytical, numerical, empirical).
3. How is machine learning used in device modeling and model parameter extraction?
4. What are the challenges in calibrating and validating device models?

L5: Evaluating

1. How is device modeling used in analog circuit design, digital circuit design, and RF circuit design?
2. What are the specific modeling requirements for power electronics devices?
3. How is device modeling used in the development of integrated circuits (ICs)?
4. What are the challenges in modeling devices for harsh environments (e.g., high temperature, radiation)?

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MTVDPE11022 **NANO-ELECTRONICS** **3 0 0 3**

Course Objectives:

1. To understand basics of Nano Electronics and the challenges due to scaling on CMOS devices
2. To understand the Carbon Nano structure and Nano MoSFET
3. To know the Data Processing for Carbon Nanotubes
4. To Know about Optical 3-D Time-of-Flight Imaging System
5. To Know about different types of sensors which are used in Realtime

At the end of the course, students will be able to:

Course Code	Course Outcomes	Mapping with POs and PSOs								Dok
		PO1	PO2	PO3	PO4	PO5	PO6	PS01	PS02	
MTVDPE11022.1	To understand and challenges due to scaling on CMOS devices	3	2	2	1	2	2	1	1	L1,L2
MTVDPE11022.2	To analyze and explain working of novel MOS based silicon devices and various multi gate devices.	3	3	3	2	1	1	2	2	L1,L2
MTVDPE11022.3	To understand working of spin electronic devices	2	2	3	1	2	2	2	3	L3,L4
MTVDPE11022.4	To understand nano electronic systems and building blocks such as: low dimensional semiconductors, hetero structures, carbon nanotubes, quantum dots, nano wires etc.	3	3	2	3	3	1	3	3	L4,L5
MTVDPE11022.5	To Understand different types of sensors which are used in real time	3	2	1	3	3	2	2	2	L4,L5

SYLLABUS

UNIT I **12 Hours**

Properties of Individual Nanoparticles: Introduction, Metal Nano Clusters, Semiconducting Nano particles, Rare Gas and Molecular Clusters, Methods of Synthesis. **COs–CO1**

UNIT II **12 Hours**

The nanoscale MOSFET, FinFETs, Vertical MOSFETs, limits to scaling, system integration limits (interconnect issues etc.), Resonant Tunnelling Transistors. Carbon Nano Structures: Introduction, Carbon Molecules, Carbon Clusters, Carbon Nano Tubes, Application of Carbon Nanotubes.

COs–CO2

UNIT III **12 Hours**

Carbon Nanotubes for Data Processing – Introduction, Electronic Properties, Synthesis of Carbon Nanotubes, Carbon Nanotube Interconnects, Carbon Nanotubes Field Effect

Transistors(CNTFETs),Nanotubes for Memory Applications, Prospects of an All-CNT Nano electronics. Neuro electronic Interfacing: Semiconductor Chips with Ion Channels, Nerve Cells, and Brain: Introduction, Iono-Electronic Interface, Neuron-Silicon Circuits, Brain-Silicon Chips.

COs–CO3

UNIT IV **12 Hours**

Optical 3-D Time-of-Flight Imaging System: Introduction, Taxonomy of Optical 3-D Techniques, CMOS Imaging, CMOS 3-D Time-of-Flight Image Sensor, Application Examples Pyroelectric Detector Arrays for IR Imaging: Introduction, Operation Principle of Pyroelectric IR Detectors, Pyroelectric Materials, Realized Devices, Characterization, and Processing Issues.

COs–CO4

UNIT V **12 Hours**

Electronic Noses: Introduction, Operating Principles of Gas Sensor Elements, Electronic Noses, Signal Evaluation, Dedicated Examples. 2-D Tactile Sensors and Tactile Sensor Arrays: Introduction, Definitions and Classifications, Resistive Touch screens, Ultrasonic Touch screens, Robot Tactile Sensors, Fingerprint Sensors. **COs–CO5**

Board of Studies : Electronics and communication Engineering
Approved in BOS No: 01, 3rd August, 2024
Approved in ACM No: 01

Text Books:

1. Introduction to Nanotechnology, C.P. Poole Jr., F.J. Owens, Wiley (2003),
2. Nano electronics and Information Technology (Advanced Electronic Materials and Novel Devices), Waser Ranier ,Wiley-VCH,2003

Reference Books:

1. Nano systems, K.E. Drexler, Wiley (1992).
2. The Physics of Low-Dimensional Semiconductors, John H. Davies, "Cambridge University Press, "1998

Web References:

1. https://onlinecourses.nptel.ac.in/noc21_mm38/preview
2. https://www.coursera.org/learn/electrical-characterization-mosfets
3. https://www.azom.com/article.aspx?ArticleID=16003

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	30	20
L2	30	30
L3	40	40
L4	--	05
L5	--	05
Total (%)	**100**	**100**

Short and Long Answers Questions of Various Cognitive Levels:

L1: Remember

1. What are Metal Nano Clusters and what are their unique properties?

2. What are Rare Gas Clusters?
3. What are the unique properties and applications of Carbon Nanotubes, and how do they differ from other carbon nanostructures like Carbon Molecules and Clusters?
4. What are the unique electronic properties of Carbon Nanotubes that make them suitable for data processing applications, and how do they differ from traditional silicon-based materials?
5. What are the unique electronic properties of Carbon Nanotubes that make them suitable for data processing applications, and how do they differ from traditional silicon-based materials?
6. What are the different types of optical 3-D techniques?
7. What is an Electronic Nose?
8. What are the different types of tactile sensors?

L2: Understand

1. How do Semiconducting Nanoparticles differ from Metal Nano Clusters in terms of their electronic properties?
2. What are Resonant Tunnelling Transistors, and how do they differ from traditional MOSFETs in terms of their operating principles and applications?
3. What is the concept of an Iono-Electronic Interface, and how can it be used to create seamless communication between semiconductor chips and biological systems like nerve cells and the brain?
4. How do CMOS 3-D Time-of-Flight Image Sensors work, and what are their advantages over other 3-D imaging technologies in terms of resolution, frame rate, and integration?
5. How does Electronic Nose mimic the human sense of smell through the use of gas sensor elements and signal evaluation techniques?

L3: Apply

1. What are some common methods of synthesizing nanoparticles, and what are their advantages and limitations?
2. What are the limitations of scaling down traditional MOSFETs, and how do FinFETs and Vertical MOSFETs address these challenges?
3. What is the operating principle of Pyroelectric IR Detectors, and how do they differ from other types of IR detectors in terms of sensitivity, speed, and power consumption?
4. How do tactile sensors vary in terms of sensing mechanism, sensitivity, and application suitability?
5. What are the key operating principles of gas sensor elements used in Electronic Noses, and how do they detect and distinguish between different odorants?

L4: Analyzing

1. How are Rare Gas Clusters synthesized?
2. What are the interconnect issues that arise in system integration at the nanoscale, and how can they be addressed through innovative materials and designs?
3. How do CNTFET offer advantages over traditional MOSFETs in terms of speed, power consumption, and scalability?
4. What are Neuron-Silicon Circuits, and how can they be used to create hybrid systems that combine the strengths of biological and electronic computing systems?
5. What are the key characteristics and challenges of Pyroelectric Materials used in IR detectors, and how do they impact the performance and reliability of the detectors?

L5: Evaluating

1. How do the optical and electrical properties of individual nanoparticles change as their size and shape are modified?
2. What are some potential applications of Carbon Nanotubes in electronics, energy storage, and biomedical fields, and what are the current challenges to their widespread adoption?
3. What are the prospects and challenges of developing an all-CNT (Carbon Nanotube) Nano electronics system, and how might it revolutionize the field of data processing and storage?
4. What are the prospects and challenges of developing an all-CNT (Carbon Nanotube) Nano electronics system, and how might it revolutionize the field of data processing and storage?
5. How Resistive and Ultrasonic Touch do screens work, and what are their advantages and limitations in terms of touch sensitivity, durability, and multi-touch capability?
6. What are some dedicated examples of Electronic Nose applications, such as quality control, environmental monitoring, and medical diagnosis, and how do they benefit from this technology?

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MTVDPE11023 **ALGORITHMS FOR VLSI DESIGN** **3 0 0 3**

Course Objectives:

1. Understand the concepts of Physical Design Process such as partitioning, Floor planning Placement and Routing.
2. Discuss the concepts of design optimization algorithms and their application to physical design automation.
3. Understand the concepts of simulation and synthesis in VLSI Design.

At the end of the course, students will be able to:

Course Code	Course Outcomes	Mapping with POs and PSOs								Dok
		PO1	PO2	PO3	PO4	PO5	PO6	PS01	PS02	
MTVDPE11023.1	Describe and formulate the flow of VLSI Design for any application.	2	1	1	1	1	0	2	1	L2,L3
MTVDPE11023.2	Explain the algorithms for floor planning, placement and routing the digital designs at frontend level & at backend VLSI Design level.	1	3	3	2	3	0	2	2	L2,L3
MTVDPE11023.3	Compare the various global routing algorithms, ILP approaches.	1	2	2	2	2	1	1	1	L1,L2
MTVDPE11023.4	Analyse single layer and three-layer detailed routing algorithms.	2	2	1	3	2	1	2	1	L4,L5
MTVDPE11023.5	Apply cell routing and minimization techniques, 1D and 2D compactions	1	3	3	2	2	1	2	1	L3,L4

SYLLABUS

UNIT–I **12 Hours**

Logic Synthesis & Verification

Introduction to Combinational Logic Synthesis, Binary Decision Diagram, Hardware Models for High-Level Synthesis.

Partitioning: Problem Formulation, Classification of Partitioning Algorithms, Group Migration Algorithms, Simulated Annealing & Evolution, other Partitioning Algorithms. **COs–CO1**

UNIT–II **12 Hours**

Placement, Floor Planning & Pin Assignment: Problem Formulation, Simulation Base Placement Algorithms, other Placement Algorithms, Constraint-Based Floor Planning, Floor Planning Algorithms for Mixed Block &Cell Design. General & Channel Pin Assignment. **COs–CO2**

UNIT–III **12 Hours**

Global Routing: Problem Formulation, Classification of Global Routing Algorithms, Maze Routing Algorithm, Line Probe Algorithm, Steiner Tree based Algorithms, ILP based Approaches.

COs–CO3

UNIT–IV **12 Hours**

Detailed Routing: Problem Formulation, Classification of Routing Algorithms, Single Layer Routing Algorithms, Two Layer Channel Routing Algorithms, Three Layer Channel Routing Algorithms, and Switchbox Routing Algorithms. **COs–CO4**

UNIT–V **12 Hours**

Over The Cell Routing & Via Minimization: Two Layers over the Cell Routers, Constrained & Unconstrained Via Minimization.

Compaction: Problem Formulation, One-Dimensional Compaction, Two Dimension - based Compaction, Hierarchical Compaction. **COs–CO5**

Board of Studies : Electrical and Electronics Engineering
Approved in BoS No: 01, 3rd August, 2024
Approved in ACM No: 01

Text Books:

1. Naveed Shervani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publisher,Second edition.
2. Christophn Meinel & Thorsten Theobold, "Algorithm and Data Structures for VLSI Design", KAP, 2002.

Reference Books:

1. Rolf Drechsheler: "Evolutionary Algorithm for VLSI", Second edition.
2. Trimburger," Introduction to CAD for VLSI", Kluwer Academic publisher, 2002.

Web References:

1. https://onlinecourses.nptel.ac.in/noc21_cs12/preview
2. https://www.coursera.org/learn/vlsi-cad-logic

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	30	30
L2	30	30
L3	30	40
L4	05	--
L5	05	--
Total (%)	**100**	**100**

Short and Long Answer Questions of Various Cognitive Levels:

L1: Remember

1. Explain the difference between ordered and reduced ordered Binary Decision Diagram
2. List different types of partitioning algorithms.
3. Describe the concept of simulation-based placement.
4. Define the global routing problem.
5. Define over-the-cell routing and its significance in modern VLSI design.

L2: Understand

1. How are BDDs used to represent Boolean functions?
2. Explain the concept of gain computation in group migration algorithms.
3. Explain the role of constraint graphs in floor planning.
4. Explain the concept of wavefront expansion.
5. Explain the potential benefits and limitations of unconstrained via minimization.

L3: Apply

1. Compare the efficiency of BDDs with other Boolean function representations.
2. Implement a simple floor planning algorithm for mixed designs.
3. Compare the performance of line probe and maze routing.
4. Implement a simple maze routing algorithm.
5. Implement a simple one-dimensional compactor for a given layout.

L4: Analyzing

1. Compare the performance of simulated annealing and genetic algorithms.
2. Analyze the complexity of solving ILP-based global routing.
3. Compare the performance of different two-layer channel routing algorithms.
4. Compare different approaches for two-dimensional compaction, such as grid-based and graph-based methods.

L5: Evaluating

1. Assess the suitability of HLS for different design applications.
2. Evaluate different pin assignment cost functions.
3. Assess the impact of Steiner tree construction on routing quality.
4. Assess the suitability of hierarchical compaction for different design styles.
5. Assess the effectiveness of one-dimensional compaction for different layout styles.

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MTMB1105 **Research Methodology and IPR** **3 0 0 3**

Course Objectives:

1. To give an overview of the research methodology and explain the technique of defining a research problem.
2. To explain the functions of the literature review in research and guide the process of conducting a literature search, reviewing it, and writing a review.
3. To explain various research designs, their characteristics, and the details of sampling designs, measurement and scaling techniques, along with different methods of data collection.
4. To explain several parametric tests of hypotheses, including the Chi-square test, and their application in research.
5. To explain various forms of intellectual property, its relevance, business impact, and leading international instruments concerning Intellectual Property Rights in the global business environment.

At the end of the course, students will be able to:

CourseCode	Course Outcomes	Mappingwith POs			Dok
		PO1	PO5	PO6	
MTMB1105.1	Understanding Research Fundamentals	2	1	2	L1,L4
MTMB1105.2	Conducting Literature Reviews	2	2	2	L1,L4
MTMB1105.3	Designing Research and Sampling Methods	3	1	2	L1,L3
MTMB1105.4	Data Collection and Analysis	3	1	2	L1,L3
MTMB1105.5	Interpreting Results and Reporting	3	3	2	L1,L4

SYLLABUS

UNIT-I: Research Methodology **10Hours**

Introduction, Meaning of Research, Objectives of Research, Types of Research, Research Approaches, Significance of Research, Research Methods versus Methodology, Research and Scientific Method, Research Process, Criteria of Good Research,. Problems Encountered by Researchers in India.

Technique Involved in Defining a Problem, an Illustration. **CO'S-CO1**

UNIT-II: Reviewing the literature **8Hours**

Place of the literature review in research, Bringing clarity and focus to research problem, Improving research methodology, Broadening knowledge base in research area, Enabling contextual findings, Review of the literature, searching the existing literature, reviewing the selected Literature, Developing a theoretical framework, Developing a conceptual framework, Writing about the literature reviewed.

Research Design: Meaning of Research Design, Need for Research Design, Features of a Good Design, Important Concepts Relating to Research Design, Different Research Designs, Basic Principles of Experimental Designs, Important Experimental Designs. **CO'S-CO2**

UNIT-III: Design of Sample Surveys **12Hours**

Design of Sampling: Introduction, Sample Design, Sampling and Non-sampling Errors, Sample

Survey versus Census Survey, Types of Sampling Designs.

Measurement and Scaling: Qualitative and Quantitative Data, Classifications of Measurement Scales, Goodness of Measurement Scales, Sources of Error in Measurement, Techniques of Developing Measurement Tools, Scaling, Scale Classification Bases, Scaling Technics, Multidimensional Scaling, Deciding the Scale.

Data, Selection of Appropriate Method for Data Collection, Case Study Method.**CO's-CO3 UNIT-IV: Testing of Hypotheses** **12Hours**

Hypothesis, Basic Concepts Concerning Testing of Hypotheses, Testing of Hypothesis, Test Statistics and Critical Region, Critical Value and Decision Rule, Procedure for Hypothesis Testing, Hypothesis Testing for Mean, Proportion, Variance, for Difference of Two Mean, for Difference of Two Proportions, for Difference of Two Variances, P-Value approach, Power of Test, Limitations of the Tests of Hypothesis. Goodness of Fit, Cautions in Using Chi Square Tests. Meaning of Interpretation, Technique of Interpretation, Precaution in Interpretation, Significance of Report Writing, Different Steps in Writing Report, Layout of the Research Report, Types of Reports, Oral Presentation, Mechanics of Writing a Research Report, Precautions for Writing Research Reports.

CO's-CO4

UNIT-V: Interpretation and Report Writing: **12Hours**

Intellectual Property: The Concept, Intellectual Property System in India, Development of TRIPS Complied Regime in India, Patents Act, 1970, Trade Mark Act, 1999, The Designs Act, 2000, The Geographical Indications of Goods(Registration and Protection) Act1999,CopyrightAct,1957, The Protection of Plant Varieties and Farmers'RightsAct,2001,TheSemi-Conductor Integrated Circuits Layout Design Act, 2000, Trade Secrets, Utility Models, IPR and Biodiversity, The Convention on Biological Diversity (CBD) 1992, Competing Rationales for Protection of IPRs, Leading International Instruments Concerning IPR, World Intellectual Property Organisation (WIPO),WIPO and WTO, Paris Convention for the Protection of Industrial Property, National Treatment, Right of Priority, Common Rules, Patents, Marks, Industrial Designs, Trade Names, Indications of Source, Unfair Competition, Patent Cooperation Treaty (PCT), Advantages of PCT Filing, Berne Convention for the Protection of Literary and Artistic Works, Basic Principles, Duration of Protection, Trade Related Aspects of Intellectual Property Rights (TRIPS) Agreement, Covered under TRIPS Agreement, Features n of the Agreement, Protection of Intellectual Property under TRIPS, Copyright and Related Rights, Trademarks, Geographical indications, Industrial Designs, Patents, Patentable Subject Matter, Rights Conferred, Exceptions, Term of protection, Conditions on Patent Applicants, Process Patents, Other Use without Authorization of the Right Holder, Layout-Designs of Integrated Circuits, Protection of Undisclosed Information, Enforcement of Intellectual Property Rights, UNSECO. **CO's-CO5**

Board of Studies : Management Science

Approved in BOS No: 05, August, 2024

Approved in ACM No: 01

Textbooks:

1. Research Methodology: Methods and Techniques - C.R. Kothari, Gaurav Garg, New Age International, 4th Edition, 2018.
2. Research Methodology a step-by-step guide for beginners. (For the topic Reviewing the literature under module2)- Ranjit Kumar SAGE Publications Ltd, 3rdEdition, 2011
3. Study Material (For the topic Intellectual Property under module5), Professional

Programme Intellectual Property Rights, Law and Practice, The Institute of Company Secretaries of India, Statutory Body under an Act of Parliament, September 2013.

Reference Books:

1. Research Methods: The concise knowledge base-Trochim, Atomic Dog Publishing,2005
2. Conducting Research Literature Reviews: From the Internet to Paper–Fink, Sage Publications, 2009.

Web References:

1. https://www.ebooksdirectory.com/
2. http://www.sciencedirect.com/Science
3. https://onlinecourses.nptel.ac.in/
4. https://www.link.springer.com/physics/
5. https://www.loc.gov/rr/scitech/selected-internet/physics.html

Internal Assessment Pattern

Cognitive Level	InternalAssessment#1(%)	InternalAssessment#2(%)
L1	30	30
L2	30	30
L3	20	20
L4	20	20
Total(%)	**100**	**100**

Sample Short and Long Answers questions of Various Cognitive Levels

Module-1: Research Methodology

1. What is the primary objective of research?
2. Describe the difference between basic and applied research.
3. Explain the significance of using the scientific method in research.
4. Differentiate between research methods and research methodology.
5. Outline the steps in the research process.
6. What are the criteria for good research?
7. Identify common problems encountered by researchers in India.
8. What are the main research approaches, and how do they differ from one another?
9. Discuss the significance of defining are search problem clearly.
10. Provide an example of how to define a research problem, including the steps involved.

Module-2: Reviewing the Literature & Research Design

1. What is the role of a literature view in a research study?
2. How does reviewing literature help in clarifying the research problem?
3. What is the difference between a theoretical frame work and a conceptual frame work?
4. List and describe the key features of a good research design.
5. Why is research design crucial for the validity of a study
6. Explain the different types of research designs and their applications?
7. What are basic principles of experimental designs?
8. How can a literature review improve research methodology?
9. Describe the process of searching and reviewing existing literature?
10. Illustrate how a well-developed theoretical framework can guide a research study?

Module-3: Design of Sample Surveys, Measurement, and Scaling

1. What is the difference between sampling errors and non-sampling errors?
2. Discuss the advantages and disadvantages of sample surveys compared to census surveys.
3. Explain the concept of sample design and its importance in research.
4. What are the classifications of measurement scales, and how are they used?
5. Describe the sources of error in measurement and techniques to minimize them.
6. Differentiate between qualitative and quantitative data.
7. What is multi dimensional scaling, and how is it applied in research?
8. Explain the process of developing a measurement tool.
9. How does scaling affect data collection and analysis?
10. Discuss the role of the case study method in data collection.

Module-4: Testing of Hypotheses

1. Define hypothesis and its role in research.
2. What is the procedure for hypothesis testing?
3. Differentiate between Type I and Type II errors in hypothesis testing.
4. Explain the concept of the critical value and its role in decision-making.
5. How do you test hypotheses for differences between two means or proportions?
6. Describe the P-value approach and its significance in hypothesis testing.
7. What is the power of a test, and why is it important?
8. Discuss the limitations of hypothesis testing.
9. Explain how the chi-square test is used for goodness of fit and its cautions.
10. Describe the different test statistics used in hypothesis testing for variances.

Module-5: Interpretation, Report Writing, and Intellectual Property

1. What is the meaning of interpretation in research, and why is it important?
2. Discuss the techniques used for interpreting research data.
3. What are the key steps in writing a research report?
4. How should a research report be structured?
5. What precautions should be taken while writing a research report?
6. Explain the concept of intellectual property and its types.
7. Discuss the TRIPS Agreement and its impact on intellectual property laws.
8. What is the role of the World Intellectual Property Organization (WIPO)?
9. How do national and international IP laws intersect?
10. Describe the protection mechanisms for patents and copyrights under Indian law.

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MTVDPC1103 **CMOS Analog IC Design Lab** **0 0 4 2**

Course Objectives:

1. Understanding CMOS Technology
2. Circuit Design and Simulation
3. Layout Design
4. Performance Analysis
5. Design Optimization and exposure to Industry Tools and Techniques

At the end of the course students will be able to:

Course Code	Course Outcomes	Mapping with POs and PSOs								Dok
		PO1	PO2	PO3	PO4	PO5	PO6	PS01	PS02	
MTVDPC1103.1	Have the ability to explain the VLSI Design Methodologies using Mentor Graphics Tools, explain the Physical Verification in Layout Design	3	2	2	1	0	0	3	3	L1,L2
MTVDPC1103.2	Grasp the significance of various CMOS analog circuits in full-custom IC Design flow, Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation	3	2	3	0	1	0	3	1	L1,L2,L3
MTVDPC1103.3	Fully Appreciate the design and analyze of analog and mixed signal simulation	3	3	3	1	1	0	2	1	L2,L3

Board of Studies : Electronics and Communication Engineering
Approved in BOS No : 01, 3rd August, 2024
Approved in ACM No : 01

List of Experiments

1. MOS Device Characterization and parametric analysis COs: CO2
2. Common Source Amplifier COs: CO2
3. Common Source Amplifier with source degeneration COs: CO2
4. Cascode amplifier COs: CO2
5. simple current mirror COs: CO2
6. Cascode current mirror. COs: CO2
7. Wilson current mirror. COs: CO2
8. Differential Amplifier COs: CO2
9. Operational Amplifier COs: CO2
10. Sample and Hold Circuit COs: CO2

11. Direct-conversion ADC COs: CO2
12. R-2R Ladder Type DAC COs: CO2

Text Books:

1. B.Razavi, "Design of Analog CMOS Integrated Circuits", 2nd Edition, McGraw Hill Edition2016.
2. Paul. R.Gray& Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits", Wiley, 5th Edition, 2009.

Reference Books:

1. T. C. Carusone, D. A. Johns & K. Martin, "Analog Integrated Circuit Design", 2nd Edition, Wiley, 2012.
2. P.E.Allen&D.R. Holberg, "CMOS Analog Circuit Design", 3rd Edition, Oxford University Press, 2011.
3. R. Jacob Baker, "CMOS Circuit Design, Layout, and Simulation", 3rd Edition, Wiley, 2010.
4. Recent literature in Analog IC Design.

Web References:

1. https://onlinecourses.nptel.ac.in/noc20_ee26/preview
2. https://www.coursera.org/specializations/chip-based-vlsi-design-for-industrial-applications

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	30	20
L2	30	40
L3	40	40
Total (%)	**100**	**100**

Lab Experiments of Various Cognitive Levels:

S. No.	Title	Cognitive Level
1	MOS Device Characterization and parametric analysis	L1, L2,L3
2	Common Source Amplifier	L1, L2,L3
3	Common Source Amplifier with source degeneration	L2,L3,
4	Cascode amplifier	L1, L2,L3
5	simple current mirror	L1, L2,L3
6	cascode current mirror	L1,L3
7	Wilson current mirror	L1, L2
8	Differential Amplifier	L1, L2,L3
9	Operational Amplifier	L1, L2,L3
10	Sample and Hold Circuit	L1, L2,L3

11	Direct-conversion ADC	L1, L2,L3
12	R-2R Ladder Type DAC	L1, L2,L3

Note: Minimum 10 Experiments to be performed.

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MTVDPC1104 **CMOS Digital IC Design Lab** **0 0 4 2**

Course Objectives:

1. Understanding CMOS Digital Design Fundamentals
2. Design of Digital Circuits
3. Circuit Simulation and Verification
4. Timing Analysis and Optimization
5. Design for Testability

At the end of the course, students will be able to:

Course Code	Course Outcomes	Mapping with POs and PSOs								Dok
		PO1	PO2	PO3	PO4	PO5	PO6	PS01	PS02	
MTVDPC1104.1	Have the ability to explain the VLSI Design Methodologies using Mentor Graphics Tools, ability to explain the Physical Verification in Layout Extraction.	2	3	2	1	0	1	3	2	L1,L2
MTVDPC1104.2	Grasp the significance of various design logic Circuits in full-custom IC Design, Pre-Layout Simulation and Post-Layout Simulation.	3	3	3	0	1	0	3	3	L1,L2,L3
MTVDPC1104.3	Fully Appreciate the design and analyze of CMOS Digital Circuits.	3	2	3	0	1	0	3	3	L3,L4

Board of Studies : Electronics and Communication Engineering
Approved in BOS No : 01, 3rd August, 2024
Approved in ACM No : 01

List of Experiments

1. Inverter Characteristics. **COs: CO2**
2. NAND and NOR Gate **COs: CO2**
3. XOR and XNOR Gate **COs: CO2**
4. 2:1 Multiplexer **COs: CO2**
5. Full Adder **COs: CO2**
6. RS-Latch **COs: CO2**
7. Clock Divider **COs: CO2**
8. JK-Flip Flop **COs: CO2**
9. Synchronous Counter **COs: CO2**
10. Asynchronous Counter COs: CO2
11. Static RAM Cell COs: CO2

12. Dynamic Logic Circuits — COs: CO2
13. Linear Feedback Shift Register — COs: CO2

Text Books:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

Reference Books:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan Borivoje Nikolic, 2nd Ed., PHI.

Web References:

1. https://onlinecourses.nptel.ac.in/noc21_ee09/preview
2. https://www.coursera.org/learn/vlsi-chip-design-and-simulation-with-electric-vlsi-eda-tool

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	30	20
L2	30	40
L3	40	40
Total (%)	**100**	**100**

Note: Minimum 10 Experiments to be performed.

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MTVDPC1205 MIXED SIGNAL & RF IC DESIGN 3 0 0 3

Course Objectives:

1. To understand the design of basic cells like Op-Amp, against process and temperature variations meeting the mixed signal specifications.
2. To be able to design comparators that can meet the high speed requirements of digital circuitry.
3. To be able to design a complete mixed signal system that includes efficient data conversion and RF circuits with minimizing switching.
4. To understand the design bottlenecks specific to RF IC design, linearity related issues, and ISI.
5. To have a comprehensive idea about different multiple access techniques, wireless standards and various transceiver architectures

At the end of the course, students will be able to:

Course Code	Course Outcomes	Mapping with POs and PSOs								Dok
		PO1	PO2	PO3	PO4	PO5	PO6	PS01	PS02	
MTVDPC1205.1	Design basic cells like Op-Amp, against process and temperature variations meeting the mixed signal specifications	2	3	2	0	1	1	2	2	L1,L2
MTVDPC1205.2	Design comparators that can meet the high speed requirements of digital circuitry.	3	3	2	1	0	1	2	2	L1,L2
MTVDPC1205.3	Design a complete mixed signal system that includes efficient data conversion and RF Circuits with minimizing switching	3	3	2	0	1	0	2	2	L3,L4
MTVDPC1205.4	Understand the design bottlenecks specific to RF IC design, linearity related issues and ISI	3	3	2	1	0	1	1	2	L1,L4,L5
MTVDPC1205.5	Comprehend different multiple access techniques, wireless standards and various transceiver architectures	3	3	2	1	1	1	2	3	L2,L3

SYLLABUS

UNIT–I: **12 Hours**

Basic Building Blocks, Op Amp, Capacitors, Switches, Non-overlapping Clocks, Basic Operation

and Analysis, Resistor Equivalence of a Switched Capacitor, Parasitic-Sensitive Integrator, Parasitic-Insensitive Integrators, Signal-Flow-Graph Analysis, Noise in Switched-Capacitor Circuit

COs–CO1

UNIT-II: **12 Hours**

Ideal D/A Converter, Ideal A/D Converter, Quantization Noise, Deterministic Approach, Stochastic Approach, Signed Codes, Performance Limitations, Resolution, Offset and Gain Error, Accuracy and Linearity Integrating Converters, Successive-Approximation Converters, DAC-Based Successive Approximation, Charge-Redistribution A/D, Resistor-Capacitor Hybrid, Speed Estimate For Charge-Redistribution Converters, Error Correction in Successive-Approximation Converters

COs–CO2

UNIT-III: **12 Hours**

Basic Phase-Locked Loop Architecture, Voltage Controlled Oscillator, Divider Phase Detector, Loop Filer, The PLL in Lock, Linearized Small-Signal Analysis, Second-Order PLL Model, Limitations of the Second-Order Small-Signal Model, PLL Design Example, Jitter and Phase Noise, Period Jitter ,P-Cycle Jitter, Adjacent Period Jitter, other Spectral Representations of Jitter, Probability Density Function of Jitter, Ring Oscillators , LC Oscillators , phase Noise of Oscillators, jitter and Phase Noise in PLLS **COs–CO3**

UNIT -IV: **12 Hours**

Introduction to RF and Wireless Technology: Complexity comparison, Design bottle necks, Applications, Analog and digital systems, Choice of Technology. BASIC CONCEPTS IN RF DESIGN: Nonlinearity and time variance, ISI, Random process and noise, sensitivity and dynamic range, passive impedance transformation **COs–CO4**

UNIT -V: **12 Hours**

Multiple Accesses: Techniques and wireless standards, mobile RF communication, FDMA, TDMA, CDMA, Wireless standards. Transceiver Architectures: General considerations, receiver architecture, Transmitter Architecture, transceiver performance tests, case studies. Amplifiers, Mixers and Oscillators: LNAs, down conversion mixers, Cascaded Stages, oscillators, Frequency synthesizers **COs–CO5&6**

Board of Studies : Electronics and Communication Engineering
Approved in BOS No: 01, 3rd August, 2024
Approved in ACM No: 01

Text Books:

1. David A Johns, Ken Martin: Analog IC design, Wiley 2008.
2. R Gregorian and G C Temes: Analog MOS integrated circuits for signal processing, Wiley 1986

Reference Books:

1. Roubik Gregorian: Introduction to CMOS Op-amps and comparators, Wiley, 2008.
2. Behzad Razavi, RF Microelectronics Prentice Hall of India, 2001
3. Thomas H. Lee, the Design of CMOS Radio Integrated Circuits, Cambridge University Press.

Web References:

1. https://ioe.iitm.ac.in/project/rf-analog-and-mixed-signal-integrated-circuits/
2. https://www.sciencedirect.com/topics/engineering/mixed-signal-integrated-circuits

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	30	10
L2	30	10
L3	40	20
L4	--	40
L5	--	20
Total (%)	**100**	**100**

Sample Short and Long Answers Questions of Various Cognitive Levels:

L1: Remember

1. What is the non-ideal characteristic of a switched capacitor integrator?
2. What kind of medium speed and high speed ADC and explain the operation of a
3. multiple-bit pipeline ADC
4. What is a basic charge pump PLL and non-ideal effects in PLLs.
5. What is RF Synthesizer Architecture

.L2: Understand

1. Explain the techniques that are adopted in a switched capacitor integrator circuit to minimize charge injection issues
2. Describe a thermometer code charge redistribution D/A converter.
3. Explain about the basic charge pump PLL with a neat figure
4. Explain the process of RF Amplifier impedance matching
5. Explain the performance of down conversion mixers and cascaded Stages

L3: Apply

1. What is an integrator using switched capacitor circuit..
2. Given a Jitter in PLLs and delay locked loops.
3. Explain is a flash converter? Discuss the working of a 3-bit flash A/D Converter
4. Given following terms with respect to mobile RF communication
5. Evaluate the performance of LNA

L4: Analysing

1. Analyze the comparison between oversampling without noise shaping and with noise shaping.
2. Analyze biquad filters. Explain about the two switched capacitor biquad realizations.
3. Analyze a 3-bit Flash ADC with quantization error centered about zero LSBs.
4. Analyze the trade-offs involved Transmitter architecture and receiver architecture.
5. A nalyze the dynamics of a simple PLL Circuit. Also explain the Jitter in PLLs and delay locked

L5: Evaluating

1. Evaluate performance of FDMA and TDMA
2. Evaluate the performance of mobile RF communications
3. What is a switched capacitor realization for a first order, high pass circuit with a high
4. frequency gain of -10 and a -3dB frequency of 1 kHz using a clock of 100kHz
5. Evaluate the dynamic characteristics that influence the performance of DACs

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MTVDPC1206 **PHYSICAL DESIGN AUTOMATION** **3 0 0 3**

Course Objectives:

1. To understand the relationship between design automation algorithms and various constraints posed by VLSI fabrication and design technology.
2. To learn the design algorithms to meet the critical design parameters.
3. To know the layout optimization techniques and map them to the algorithms
4. To understand proto-type EDA tools and know how to test its efficacy

At the end of the course, students will be able to:

Course Code	Course Outcomes	Mapping with POs and PSOs								Dok
		PO1	PO2	PO3	PO4	PO5	PO6	PS01	PS02	
MTVDPC1206.1	Understand the relationship between design automation algorithms and Various constraints	3	3	1	3	1	2	2	2	L1,L2
MTVDPC1206.2	Posed by VLSI fabrication and design technology.	2	2	2	3	3	2	3	3	L1,L2
MTVDPC1206.3	Adapt the design algorithms to meet the critical design parameters.	3	3	3	2	2	2	3	3	L3,L4
MTVDPC1206.4	Identify layout optimization techniques and map them to the algorithms	2	3	3	3	3	2	3	3	L3,L4
MTVDPC1206.5	Understand the algorithms in partitioning, routing and Placement	2	2	3	2	2	2	2	2	L4,L5

SYLLABUS

UNIT –I: **12 Hours**

VLSI design Cycle, Physical Design Cycle, Design Rules, Layout of Basic Devices, and Additional Fabrication, Design styles: full custom, standard cell, gate arrays, field programmable gate arrays, sea of gates and comparison, system packaging styles, multi-chip modules. Design rules, layout of basic devices, fabrication process and its impact on physical design, interconnect delay, noise and cross talk, yield and fabrication cost. **COs–CO1**

UNIT -II: **12 Hours**

Factors, Complexity Issues and NP-hard Problems, Basic Algorithms (Graph and Computational Geometry): graph search algorithms, spanning tree algorithms, shortest path algorithms, matching algorithms, min-cut and max-cut algorithms, Steiner tree algorithms **COs–CO2**

UNIT -III: **12 Hours**

Basic Data Structures, atomic operations for layout editors, linked list of blocks, bin based methods, neighbour pointers, corner stitching, multi-layer operations. **COs–CO3**

UNIT -IV: **12 Hours**

Graph algorithms for physical design: classes of graphs, graphs related to a set of lines, graphs related to set of rectangles, graph problems in physical design, maximum clique and minimum coloring, maximum k-independent set algorithm, algorithms for circle graphs. **COs–CO4**

UNIT -V: **12 Hours**

Partitioning algorithms: design style specific partitioning problems, group migrated algorithms, simulated annealing and evolution, and Floor planning and pin assignment, Routing and placement Algorithms **COs–CO5**

Board of Studies : Electronics and Communication Engineering
Approved in BOS No: 01, 3rd August, 2024
Approved in ACM No: 01

Text Books:

1. Naveed Shervani, Algorithms for VLSI Physical Design Automation, 3rd Edition, Kluwer Academic, 1999.
2. Charles J Alpert, Dinesh P Mehta, Sachin S Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press, 2008

Web References:

1. https://nptel.ac.in/courses/117106092
2. https://onlinecourses.nptel.ac.in/noc24_cs70/preview
3. https://en.wikipedia.org/wiki/Very-large-scale_integration

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	30	20
L2	30	30
L3	40	40
L4	--	05
L5	--	05
Total (%)	**100**	**100**

Sample Short and Long Answers Questions of Various Cognitive Levels:

L1: Remember

1. What are the key stages involved in the VLSI design cycle, and how do they interact to ensure a successful chip design?
2. What are NP-hard problems?
3. What is the Steiner tree problem?
4. How do algorithms like the Steiner tree approximation algorithm or the exact algorithm for Steiner trees solve Steiner tree problem?
5. What are atomic operations in the context of layout editors?

L2: Understand

1. What are the main design rules and constraints that must be considered during the physical design cycle to ensure correct functionality and manufacturability?
2. How do NP-hard problems differ from NP-complete problems in terms of their computational complexity and solvability?

3. Describe the basic steps and complexity of the Hopcroft-Karp algorithm for finding maximum cardinality matchings in bipartite graphs, and how it differs from other matching algorithms
4. What are the advantages and disadvantages of using a linked list of blocks to represent a layout in a layout editor, compared to other data structures like arrays or trees?
5. What are the advantages and disadvantages of using a linked list of blocks to represent a layout in a layout editor, compared to other data structures like arrays or trees?

L3: Apply

1. Compare and contrast the different design styles (full custom, standard cell, gate arrays, field programmable gate arrays, sea of gates) in terms of their advantages, disadvantages, and application suitability.
2. Tabulate Steiner tree problem complexity and limitations?
3. How do pointers and corner stitching enable efficient traversal and modification of the layout data structure, particularly in multi-layer layouts?
4. How are graphs related to a set of lines, such as intersection graphs and visibility graphs, used to model physical design problems like wire routing and placement?
5. Compare and contrast routing and placement algorithms, such as maze routing and force directed placement, in terms of their objectives, constraints, and application suitability.

L4: Analysing

1. Differenciate between Dijkstra's algorithm and Bellman-Ford algorithm for finding shortest paths in graphs, and how do they handle negative weight edges?
2. What are some common graph problems that arise in physical design, such as maximum clique, minimum coloring, and maximum k-independent set, and how are they applied to physical design optimization?
3. What are the key considerations and algorithms for floor planning and pin assignment in physical design, and how do they impact the overall quality of the design?
4. Analyze how do context of layout editors ensure consistency and correctness when modifying the layout data structure?

L5: Evaluating

1. What are the key factors that affect yield and fabrication cost in VLSI design, and how can designers optimize their designs to improve these metrics?
2. What are the challenges and considerations when performing operations on multi-layer layouts and how can data structures and algorithms be optimized to handle these complexities?
3. What are some algorithms for solving graph problems on circle graphs, such as recognition, coloring, and clique finding, and how are they applied to physical design problems like routing and placement?

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MTVDPE12031 **VLSI SIGNAL PROCESSING** **3 0 0 3**

Course Objectives:

1. To Understand the existing or new DSP architectures suitable for VLSI
2. To understand the concepts of folding and unfolding algorithms.
3. To learn the concepts of Systolic Architecture.
4. To learn and implement fast convolution algorithms..
5. To understand the Low power design aspects of processors for signal processing.

At the end of the course, students will be able to:

Course Code	Course Outcomes	Mapping with POs and PSOs								Dok
		PO1	PO2	PO3	PO4	PO5	PO6	PS01	PS02	
MTVDPE12031.1	Ability to modify the existing or new DSP architectures suitable for VLSI.	2	2	2	1	1	1	3	2	L1,L2
MTVDPE12031.2	Understand the concepts of folding and unfolding algorithms and applications.	3	2	3	2	2	2	1	3	L1,L2
MTVDPE12031.3	Understand the concepts of Systolic Architecture Design	3	2	3	1	2	2	3	1	L3,L4
MTVDPE12031.4	Ability to implement fast convolution algorithms.	3	2	2	2	2	1	3	1	L4,L5
MTVDPE12031.5	Understand the Low power design aspects of processors for signal processing and wireless applications.	3	2	3	3	3	2	3	1	L1,L2

SYLLABUS

UNIT–I: **12 Hours**

Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms Pipelining and Parallel Processing, Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques. **COs–CO1**

UNIT–II: **12 Hours**

Folding and Unfolding: Folding- Introduction, Folding Transform, Register minimization Techniques, Register minimization in folded architectures, folding of Multirate systems Unfolding- Introduction, An Algorithm for Unfolding, Properties of Unfolding, critical Path, Unfolding and Retiming, Applications of Unfolding. **COs–CO2**

UNIT–III: **12 Hours**

Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations contain Delays. **COs–CO3**

UNIT–IV: **12 Hours**

Fast Convolution: Introduction–Cook-Toom Algorithm–Winogard algorithm–Iterated Convolution – Cyclic Convolution–Design of Fast Convolution algorithm by Inspection. **COs–CO4**

UNIT-V: **12 Hours**

Digital lattice filter structures, bit level arithmetic, architecture, redundant arithmetic. Numerical strength reduction, synchronous, wave and asynchronous pipe lines, low power design. Low Power Design: Scaling Vs Power Consumption, Power Analysis, Power Reduction techniques, Power Estimation Approaches **COs–CO5**

Board of Studies : Electronics and Communication Engineering
Approved in BOS No: 01, 3rd August, 2024
Approved in ACM No: 01

Text Books:

1. Keshab K. Parthi[A1] , VLSI Digital signal processing systems, design and implementation[A2] Wiley, Inter Science, 1999.
2. Mohammad Isamail and Terri Fiez, Analog VLSI signal and information processing, McGraw Hill, 1994
3. S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing, Prentice Hall, 1985.

Web References:

1. https://archive.nptel.ac.in/courses/108/105/108105157/

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	30	20
L2	30	30
L3	40	40
L4	--	05
L5	--	05
Total (%)	**100**	**100**

Sample Short and Long Answers Questions of Various Cognitive Levels:

L1: Remember

1. What are the different types of DSP algorithms?
2. Explain the concept of retiming.
3. Define terms like critical path, iteration bound, loop bound.
4. What are the different types of digital filters?
5. Define pipelining and parallel processing.

L2: Understand

1. How does pipelining improve performance in DSP systems?
2. Explain the benefits of parallel processing in DSP.
3. What is the role of retiming in low-power design?
4. How are DSP algorithms represented for hardware implementation?
5. What is the connection between DSP algorithms and filter design?

L3: Apply

1. Design a parallel processing architecture for a specific DSP algorithm.
2. How would you use retiming to reduce power consumption in a given circuit?
3. Given a DSP algorithm, how would you choose an appropriate representation for hardware implementation?
4. What is the trade-offs between pipelining and parallel processing?

L4: Analysing

1. Analyze the impact of data dependencies on parallel processing efficiency.
2. Evaluate the effectiveness of retiming techniques for different circuit topologies.
3. Compare different DSP algorithm representations in terms of area, power, and performance.
4. How does increasing the pipeline stages affect latency and throughput?
5. What is the impact of data hazards on parallel processing?

L5: Evaluating

1. Evaluate the suitability of different DSP algorithms for a given application.
2. Assess the trade-offs between performance, power, and area for various pipelining and parallel processing strategies.
3. Critique the effectiveness of retiming techniques in different design scenarios.
4. Determine the optimal DSP algorithm representation for a target hardware platform.

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MTVDPE12032 **IOT & ITS APPLICATIONS** **3 0 0 3**

Course Objectives:

1. Apply the Knowledge in IOT Technologies and Data management.
2. Determine the values chains Perspective of M2M to IOT.
3. Implement the state of the Architecture of an IOT.
4. Compare IOT Applications in Industrial & real world.
5. Demonstrate knowledge and understanding the security and ethical issues of an IOT.

At the end of the course, students will be able to:

Course Code	Course Outcomes	Mapping with POs and PSOs								Dok
		PO1	PO2	PO3	PO4	PO5	PO6	PS01	PS02	
MTVDPE12032.1	Introduction to IOT and WEB technologies	3	2	2	0	1	2	3	3	L1,L2,L3
MTVDPE12032.2	Understand the concept of IOT and M2M	3	3	2	1	2	1	2	3	L2,L3
MTVDPE12032.3	Study IOT architecture	3	3	2	1	1	1	3	3	L1,L3
MTVDPE12032.4	Applications in various fields	3	3	3	1	2	2	3	3	L3,L4
MTVDPE12032.5	Study the security and privacy issues in IOT.	3	3	3	1	0	0	2	3	L4,L5

SYLLABUS

UNIT I: Fundamentals of IoT **12 Hours**

Evolution of Internet of Things, Enabling Technologies, IoTArchitectures,oneM2M, IoT World Forum (IoTWF) and Alternative IoT models, Simplified IoT,Architecture and Core IoT Functional Stack, Fog, Edge and Cloud in IoT, Functional blocks of an IoT ecosystem, Sensors, Actuators, Smart Objects and Connecting Smart Objects. IoT Platform overview: Overview of IoT supported Hardware platforms such as: Raspberry pi, ARM Cortex Processors, Arduino and Intel Galileo boards. **COs–CO1**

UNIT II: IoT Protocols **12 Hours**

IT Access Technologies: Physical and MAC layers, topology and Security of IEEE 802.15.4, 802.15.4g, 802.15.4e, 1901.2a, 802.11ah and Lora WAN, Network Layer: IP versions, Constrained Nodes and Constrained Networks, Optimizing IP for IoT: From 6LoWPAN to6Lo, Routing over Low Power and Lossy Networks, Application Transport Methods: Supervisory Control and Data Acquisition, Application Layer Protocols: CoAP and MQTT. **COs–CO2**

UNIT III: Design And Development **12 Hours**

Design Methodology, Embedded computing logic,Microcontroller, System on Chips, IoT system building blocks, Arduino, Board details, IDE programming, Raspberry Pi, Interfaces and Raspberry Pi with Python Programming. **COs–CO3**

UNIT IV: Data Analytics And Supporting Services **12 Hours**

Structured Vs Unstructured Data and Data in Motion Vs Data in Rest, Role of Machine Learning – No SQL Databases, Hadoop Ecosystem, Apache Kafka, Apache Spark, Edge Streaming Analytics and Network Analytics, Xively Cloud forIoT, Python Web Application Framework, Django, AWS for IoT, System Management with NETCONF-YANG **COs–CO4**

UNIT V: Case Studies/Industrial Applications: **12 Hours**

IoT applications in home, infrastructures, buildings, security, Industries, Home appliances, other IoT electronic equipments. Use of Big Dataand Visualization in IoT, Industry 4.0 concepts. Sensors and sensor Node and interfacing using any Embedded target boards (Raspberry Pi / Intel Galileo/ARM Cortex/ Arduino) **COs–CO5**

Board of Studies : Electronics and Communication Engineering
Approved in BOS No: 01, 3rd August, 2024
Approved in ACM No: 01

Text Books:

1. 1.IoT Fundamentals: Networking Technologies, Protocols and Use Cases for Internet of Things,David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Rob Barton and Jerome Henry, Cisco Press, 2017

Reference Books:

1. Internet of Things – A hands-on approach, ArshdeepBahga, Vijay Madisetti, UniversitiesPr.
2. The Internet of Things – Key applications and Protocols, Olivier Hersent, David Boswarthick,Omar Elloumi and Wiley, 2012 (for Unit 2).
3. "From Machine-to-Machine to the Internet of Things – Introduction to a New Age of
4 Intelligence",Jan Ho¨ ller, VlasiosTsiatsis, Catherine Mulligan, Stamatis, Karnouskos, Stefan
5. Avesand. David Boyle and Elsevier, 2014.
6. 4. Architecting the Internet of Things,Dieter Uckelmann, Mark Harrison, Michahelles and Florian(Eds), Springer, 2011.
6. Recipes to Begin, Expand, and Enhance Your Projects, 2nd Edition,Michael Margolis, Arduino Cookbook and O"Reilly Media, 2011.

Web References:

1. https://www.edx.org/learn/iot-internet-of-things
2. https://onlinecourses.nptel.ac.in/noc19_cs65/preview
3. https://www.coursera.org/in/articles/internet-of-things

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	30	20
L2	30	30
L3	40	40
L4	--	05
L5	--	05
Total (%)	**100**	**100**

Sample Short and Long Answers Questions of Various Cognitive Levels:

L1: Remember

1. Explain the key drivers of IoT growth and development.
2. Define IP, IPv4, IPv6, and constrained networks.
3. Define embedded computing, microcontroller, and SoC.

4. Define NoSQL, Hadoop, Kafka, and Spark.
5. Define IoT and its key components.

L2: Understand

1. Explain the role of cloud computing in IoT.
2. Explain the role of application layer protocols in IoT.
3. Explain the role of Arduino in IoT development
4. Explain the role of cloud platforms in IoT solutions.
5. Explain the role of data analytics in IoT.

L3: Apply

1. Design a simple IoT architecture for a home automation system.
2. Configure IP settings for a constrained IoT device.
3. Use Python to control GPIO pins on a Raspberry Pi.
4. Develop a simple IoT application using Python and Django.
5. Identify Industry 4.0 use cases in manufacturing.

L4: Analysing

1. Compare oneM2M with other IoT standards and frameworks.
2. Compare and contrast the features of IEEE 802.15.4 variants (e.g., 802.15.4g, 802.15.4e).
3. Compare different Arduino boards based on their features and specifications.
4. Compare and contrast traditional databases with NoSQL databases.
5. Compare and contrast traditional manufacturing with Industry 4.0.

L5: Evaluating

1. Assess the impact of fog and edge computing on IoT scalability and performance.
2. Assess the impact of IoT platforms on the development of IoT applications.
3. Assess the suitability of Raspberry Pi for different IoT applications.
4. Assess the security and privacy implications of cloud-based IoT solutions.
5. Assess the impact of sensor accuracy and precision on IoT applications.

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MTVDPE12033 **PHYSICS OF VLSI DEVICES** **3 0 0 3**

Course Objectives:

1. Explain the fundamentals of intrinsic, extrinsic semiconductors with carrier concentration, modeling and physics of various carrier current transport mechanisms
2. Introduce detailed physics and modeling of PN Junction, MOS capacitors, and MOSFETs
3. Review and discuss in detail the short channel effects and the issues of UDSM transistors

At the end of the course, students will be able to:

Course Code	Course Outcomes	Mapping with POs and PSOs								Dok
		PO1	PO2	PO3	PO4	PO5	PO6	PS01	PS02	
MTVDPE12033.1	Design extrinsic semiconductors with specific carrier concentrations and, understand the band structure and diagrams of semiconductors.	3	3	2	0	0	1	3	2	L4,L5
MTVDPE12033.2	Calculate and model the carrier transport mechanism in semiconductors.	3	2	2	0	1	1	2	2	L3,L4,L5
MTVDPE12033.3	Model PN- junctions of given specifications	3	2	2	1	0	1	2	3	L2,L3
MTVDPE12033.4	Model MOS capacitors and Model MOSFETs	2	3	3	1	0	1	2	1	L2,L4
MTVDPE12033.5	Mitigate the short channel effects and design UDSM transistors	2	2	1	1	1	1	1	1	L1,L4,L5

SYLLABUS

UNIT–I: Semiconductor Physics and Carrier Transport in Semiconductors **12 Hours**

Energy bands in solids - Intrinsic and Extrinsic semiconductors - Direct and Indirect bandgap - Density of states - Fermi distribution -Free carrier densities - Boltzmann statistics - Thermal equilibrium. Current flow mechanisms: Drift current, Diffusion current - Mobility of carriers - Current density equations - Continuity equation. **COs–CO1**

UNIT–2: P-N Junctions **12 Hours**

Thermal equilibrium physics - Energy band diagrams - Space charge layers - Poisson equation - Electric fields and Potentials - p-n junction under applied bias - Static current-voltage characteristics of p-n junctions - Breakdown mechanisms. **COs–CO2**

UNIT –3: MOS Capacitor and MOSFETs and Compact Models **12 Hours**

Accumulation - Depletion - Strong inversion - Threshold voltage - Contact potential - Gate work function - Oxide and Interface charges - Body effect - C-V characteristics of MOS Drain current - Saturation voltage - Sub-threshold conduction - Effect of gate and drain voltage on carrier mobility - Compact models for MOSFET and their implementation in SPICE: Level 1, 2 and 3 - MOS model parameters in SPICE. **COs–CO3**

UNIT–4: Scaling and Short Channel Effects **12 Hours**

Effect of scaling - Channel length modulation - Punch-through - Hot carrier degradation - MOSFET breakdown - Drain-induced barrier lowering. **COs–CO4**

UNIT–5:UDSM Transistor Design Issues **12 Hours**

Effect of tox - Effect of high-k and low-k dielectrics on the gate leakage and Source and drain leakage - tunneling effects - Different gate structures in UDSM - Impact and reliability challenges in UDSM. **COs–CO5**

Board of Studies : Electronics and Communication Engineering
Approved in BOS No: 01, 3rd August, 2024
Approved in ACM No: 01

Text Books:

1. Ben G. Streetman and S. Banerjee, Solid State Electronic Devices, Pearson Education, U.S, Seventh Edition, 2014.
2. J.P. Colinge and C. A. Colinge, Physics of Semiconductor Devices, Kluwer Academic Publishers, US, 2017.

Reference Books:

1. Y.P. Tsividis and Colin McAndrew, Operation and Modelling of the MOS Transistor, Oxford University Press, US, Third Edition, 2011.
2. M K Achutan and K N Bhatt, Fundamental of Semiconductor Devices, McGraw Hill Education, US, 2017.

Web References:

1. https://onlinecourses.nptel.ac.in/noc22_ee97/preview
2. https://www.coursera.org/learn/semiconductor-physics

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	30	20
L2	30	30
L3	40	40
L4	--	05
L5	--	05
Total (%)	**100**	**100**

Sample Short and Long Answers Questions of Various Cognitive Levels:

L1: Remember

1. What is the difference between intrinsic and extrinsic semiconductors?
2. What is the Fermi-Dirac distribution function?
3. What is the threshold voltage, and how does it affect MOSFET operation?
4. What is channel length modulation and how does it affect the MOSFET's I-V characteristics?

L2: Understand

1. Describe the effect of doping on the electronic properties of a semiconductor.
2. Explain the concept of the depletion region in a p-n junction.
3. Describe the body effect and its impact on the threshold voltage.

4. Explain how scaling affects the threshold voltage and drive current of a MOSFET.
5. How does decreasing gate oxide thickness affect the threshold voltage and the drive current of a MOSFET?

L3: Apply

1. Determine the current density for a semiconductor device under a given electric field and carrier concentration.
2. Calculate the drain current for a given gate and drain voltage using the MOSFET equation in saturation mode.
3. Given a MOSFET with a specified channel length modulation parameter (λ), calculate the change in drain current for a given increase in drain-to-source voltage.
4. Given a MOSFET with a specified gate oxide thickness, calculate the impact on the gate capacitance and subthreshold leakage current if toxt_{ox}tox is reduced.

L4: Analysing

1. Analyze the impact of temperature on the conductivity of intrinsic semiconductors.
2. Analyze how different doping levels affect the width of the depletion region and the breakdown mechanisms in a p-n junction.
3. Compare the C-V characteristics of a MOS capacitor in accumulation, depletion, and inversion regions.
4. Analyze the effect of scaling on the short-channel effects and how it impacts MOSFET performance in modern integrated circuits.
5. Analyze the trade-offs involved in reducing gate oxide thickness, including impacts on leakage currents and breakdown voltage.

L5: Evaluating

1. Evaluate the performance of a semiconductor device based on its mobility and carrier density
2. Evaluate the performance of a p-n junction diode based on its current-voltage characteristics and breakdown mechanisms.
3. Assess the impact of gate and drain voltage on carrier mobility and how it affects the MOSFET's switching characteristics.
4. Evaluate the performance of a MOSFET in terms of punch-through and hot carrier degradation under various operating conditions.
5. Evaluate the overall impact of gate oxide thickness changes on the reliability and performance of MOSFETs in an integrated circuit.

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MTVDPE12041 EMBEDDED SYSTEM DESIGN 3 0 0 3

Course Objectives:

1. To introduce the Building Blocks of Embedded System.
2. To Educate in Various Embedded Development Strategies.
3. To Introduce Bus Communication in processors, Input/output interfacing.
4. To impart knowledge in various processor scheduling algorithms.
5. To introduce Basics of Real time operating system and example tutorials to discuss on one real time operating system tool.

At the end of the course, students will be able to:

Course Code	Course Outcomes	Mapping with POs and PSOs								Dok
		PO1	PO2	PO3	PO4	PO5	PO6	PS01	PS02	
MTVDPE12041.1	Acquire basic knowledge about fundamentals of microcontrollers	2	2	3	2	2	2	3	3	L1,L2
MTVDPE12041.2	Acquire basic knowledge about programming and system control to perform specific task.	3	2	2	3	3	2	3	3	L1,L2,L3
MTVDPE12041.3	Acquire knowledge about devices and buses used in Embedded networking.	3	2	3	3	3	2	3	2	L3,L4
MTVDPE12041.4	Develop programming skills in embedded systems for various applications	3	3	3	2	3	3	3	3	L4,L5
MTVDPE12041.5	Acquire knowledge about basic concepts of circuit emulators and life cycle of embedded design and its testing	3	3	2	2	2	1	2	2	L2,L3,L5

SYLLABUS

UNIT–I: 12 Hours

Introduction to Embedded Electronic Systems and Microcontrollers:

An Embedded System-Definition, Embedded System Design and Development Life Cycle, An Introduction to Embedded system Architecture, The Embedded Systems Model, Embedded Hardware: The Embedded Board and the von Neumann Model, Embedded Processors: ISA Architecture Models, Internal Processor Design, Processor Performance, Board Memory: Read-Only Memory (ROM), Random-Access Memory (RAM), Auxiliary Memory, Memory Management of External Memory and Performance, Approaches to Embedded Systems, Small

Microcontrollers, Anatomy of a Typical Small Microcontroller, Small Microcontrollers Memory, Embedded Software, Introduction to small microcontroller (MSP430). **COs–CO1**

UNIT-II: MSP430–I **12 Hours**

Architecture of the MSP430 Processor: Central Processing Unit, Addressing Modes, Constant Generator and Emulated Instructions, Instruction Set, Examples, Reflections on the CPU and Instruction Set, Resets, Clock System, Memory and Memory Organization.

Functions, Interrupts, and Low-Power Mode: Functions and Subroutines, Storage for Local Variables, Passing Parameters to a Subroutine and Returning a Result, Mixing C and Assembly Language, Interrupts, Interrupt Service Routines, Issues Associated with Interrupts, Low-Power Modes of Operation. **COs–CO2**

UNIT–III: MSP430–II **12 Hours**

Digital Input, Output, and Displays: Parallel Ports, Digital Inputs, Switch Debounce, Digital utputs, Interface between Systems, Driving Heavier Loads, Liquid Crystal Displays, Simple Applications of the LCD.

Timers: Watchdog Timer, Timer_A, Timer_A Modes, Timer_B,Timer_B Modes, Setting the Real-Time Clock, State Machines. **COs–CO3**

UNIT–IV: MSP430 Communication **12 Hours**

Communication Peripherals in the MSP430, Serial Peripheral Interface, SPI with the USI, SPI with the USCI, AThermometer Using SPI Modes,Inter-integrated Circuit Bus(I^2C) and its operations, State Machines for I^2C Communication, AThermometer Using I^2C, Asynchronous Serial Communication, Asynchronous Communication with the USCI_A, ASoftware UART Using Timer_A, Other Types of Communication. **COs–CO4**

UNIT–V: MSP430 Case Studies **12 Hours**

Introduction to Code Composer studio (CC Studio Ver. 6.1) a tutorial, A Study of blinking LED, Enabling LED using Switches, UART Communication, LCD interfacing, Interrupts, Analog to Digital Conversion, General Purpose input and output ports, I2C. **COs–CO5**

Board of Studies : Electrical and Electronics Engineering
Approved in BOS No: 01, 23rd July, 2024
Approved in ACM No:

Text Books:

1. Tammy Noergaard "Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers", Elsevier(Singapore) Pvt.Ltd.Publications, 2005.
2. John H. Davies "MSP430 Microcontroller Basics",Elsevier Ltd Publications, Copyright 2008.

Reference Books:

1. Manuel Jiménez Rogelio,PalomeraIsidoro Couvertier "Introduction to Embedded Systems Using Microcontrollers and the MSP430" Springer Publications, 2014.
2. Frank Vahid, Tony D. Givargis, "Embedded system Design: A Unified Hardware/Software Introduction", John Wily & Sons Inc.2002.
3. Peter Marwedel, "Embedded System Design", Science Publishers, 2007.
4. Arnold S Burger, "Embedded System Design", CMP Books, 2002.
5. Rajkamal, "Embedded Systems: Architecture, Programming and Design", TMH Publications, Second Edition, 2008.

Web References:

1. https://en.wikipedia.org/wiki/Embedded_system

2. https://onlinecourses.nptel.ac.in/noc20_ee98/preview

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	30	20
L2	30	10
L3	40	20
L4	--	30
L5	--	20
Total (%)	**100**	**100**

Sample Short and Long Answers Questions of Various Cognitive Levels:

L1: Remember

1. What is an embedded system? What are the components of embedded system?
2. What are the functions of memory?
3. How does interrupt system of MSP430 work?
4. What are state machines in MSP430 – II
5. What is bit bagging?

L2: Understand

1. Describe functions of memory?
2. Describe the architecture of MSP430?
3. Explain the operation of watchdog timer?
4. Illustrate the operation of SPI with USCI?
5. Summarize the operation of SPI with USI?

L3: Apply

1. Draw and compare von-Neumann and Harvard architecture.
2. Explain the memory architecture of MSP430?
3. How MSP430 drives heavy loads?
4. Explain the concept of synchronous and asynchronus communication using MSP430
5. Explain the operation of blinking LED?

L4: Analyzing

1. Analyze the working of interrupt system of MSP430 work?
2. Develop steps for the usage of ADC in MSP430?
3. Analyze different modes of timers in MSP430 – II?
4. How do we perform UART communication in MSP430?
5. Compare different timers in MSP430-II?

L5: Evaluating

1. Propose a model for interfacing the LCD with MSP430
2. Construct a Analog to digital converter using MSP430-II
3. Elaborate the operation of state machines in MSP430 – I
4. Derive a model which uses ADC and LED?
5. Differentiate MSP430-I and MSP430-II?

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MTVDPE12042 Microcontrollers & Programmable Digital Signal Processors 3 0 0 3

Course Objectives:

1. To learn about ARM Cortex-M3 Processor
2. To learn about Timers & Interrupts
3. To understand the 17xx Microcontroller Architecture and Memory arrangement
4. To Understand the Programmable DSP architectural Structure
5. To learn about VLIW architecture and System on chip

At the end of the course, students will be able to:

Course Code	Course Outcomes	Mapping with POs and PSOs								Dok
		PO1	PO2	PO3	PO4	PO5	PO6	PSO 1	PSO 2	
MTVDPE12042.1	Introduction to Cortex-M3 Processor	3	2	3	1	3	2	3	3	L1, L2, L3
MTVDPE12042.2	Understand the concept of Timers and Interrupts	3	2	2	2	3	2	2	2	L2, L3
MTVDPE12042.3	Study 17xx memory arrangement	3	2	2	2	3	1	1	2	L1, L3
MTVDPE12042.4	Understand the Programmable DSP architectural Structure	3	1	3	3	3	2	2	3	L4, L3
MTVDPE12042.5	Study the VLIW architecture and system on chip OT.	3	1	3	3	3	2	2	3	L4, L5

SYLLABUS

UNIT 1: **12 Hours**

ARM Cortex-M3 processor: Applications, Programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces. **COs–CO1**

UNIT 2: **12 Hours**

Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behaviour, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency. **COs–CO2**

UNIT 3: **12 Hours**

LPC 17xx microcontroller- Internal memory, GPIOs, Timers, ADC, UART and other Serial interfaces, PWM, RTC, WDT. **COs–CO3**

UNIT 4: **12 Hours**

Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory, architectural structure of P-DSP- MAC unit, Barrel shifters, Introduction to TI DSP processor family **COs–CO4**

UNIT 5: **12 Hours**

VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths,

Introduction to Instruction level architecture of C6000 family, Assembly Instructions Memory addressing, for arithmetic, logical operations Code Composer Studio for application development for digital signal processing, On chip peripherals, Processor benchmarking. **COs–CO5**

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Text Books:

1. Joseph Yiu, "The definitive guide to ARM Cortex-M3", Elsevier, 2nd Edition
2. Venkatramani B. and Bhaskar M. "Digital Signal Processors: Architecture, Programming and Applications" , TMH , 2nd Edition
3. Sloss Andrew N, Symes Dominic, Wright Chris, "ARM System Developer's Guide: Designing and Optimizing", Morgan Kaufman Publication

Reference Books:

1. Steve furber, "ARM System-on-Chip Architecture", Pearson Education
2. Frank Vahid and Tony Givargis, "Embedded System Design", Wiley
3. Technical references and user manuals on www.arm.com, NXP Semiconductorwww.nxp.com and Texas Instruments www.ti.com

Web References:

1. https://nptel.ac.in/courses/117104072
2. https://www.slideshare.net/slideshow/micro-controller-and-dsp-processor 121078191 / 121078191
3. https://onlinecourses.nptel.ac.in/noc24_ee46/preview

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	30	30
L2	30	20
L3	40	30
L4	--	10
L5	--	10
Total (%)	**100**	**100**

Sample Long Answers questions of Various Cognitive Levels

L1: Remember

1. What is meant by research Instruction set? Explain the pipeline and Bus interface concept
2. What is meant by Nested Interrupt Control and explain about an Interrupt
3. Show the serial Interfaces of LPC 17xx Micro Controller with a neat sketch
4. Define the Architectural structure of Programmable DSP –MAC unit
5. List the Assembly Instructions and Memory Addressing for Arithematic and Logical Operations

L2: Understand

1. Explain the Memory Access attributes and Permissions in ARM Cortex M3 Processor
2. Demonstrate the basic configuration of SYSTIC Timer
3. Illustrate the architecture of UART and PWM
4. Show how the Barrel Shifters work
5. Outline the On chip Peripherals and Processor Bench marking

L3: Apply

1. Develop a program with Reset Sequence Instruction set
2. Explain about fault exceptions and make use of it in real time.
3. Utilize the exceptions, types, priority, vector tables of Cortex M3 Processor
4. Make use of RTC and WDT in M3 Processor
5. Model the multiport memory of Programmable DSP Processors
6. Make use of Code Composer Studio for application Development for DSP

L4: Analysing

1. List out the Registers, operation modes, Exceptions and Interrupts
2. Categorize the Interrupt Sequences and Interrupt latency
3. Distinguish ADC and Timers in LPC 17xx Microcontroller
4. Conclude the Processor Bench marking with a neat sketch
5. Contrast Harvard and Von-Neumann Architecture

L5: Evaluating

1. Explain about Supervisor and Pendable Service Call
2. Determine the T1 DSP Processor Family
3. Explain about LPC 17xx Microcontroller GPIO's
4. Perceive the VLIW architecture and TMS320C6000 series
5. Explain about ARM Cortex-M3 Processor Programming Model and list out the Applications

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MTVDPE12043 LOW POWER VLSI DESIGN 3 0 0 3

Course Objectives:

1. Describe switching power dissipation and its relationship with dynamic power consumption in digital circuits.
2. Understand the concept of voltage swing and its effect on power dissipation in digital circuits.
3. Explain the concept of pipelining and its impact on power consumption by improving instruction throughput while maintaining low power usage.
4. Understand One-Hot coding and how it represents each state of a bus with a single active bit.
5. Define data correlation in the context of Digital Signal Processing (DSP) systems and its impact on power analysis.

At the end of the course, students will be able to:

Course Code	Course Outcomes	Mapping with POs and PSOs								Dok
		PO1	PO2	PO3	PO4	PO5	PO6	PS01	PS02	
MTVDPE12043.1	Identify the sources of power dissipation in digital IC systems & understand the impact of power on system performance and reliability.	2	2	1	1	1	0	2	1	L2, L3
MTVDPE12043.2	Characterize and model power consumption & understand the basic analysis methods.	2	2	1	1	1	1	2	2	L1, L2
MTVDPE12043.3	Understand leakage sources and reduction techniques.	2	1	2	1	0	0	2	2	L2, L3
MTVDPE12043.4	Understand the concept of glitching in digital circuits and its impact on power consumption.	1	2	3	0	1	0	2	1	L2, L4
MTVDPE12043.5	Understand and apply timing analysis techniques to verify the timing characteristics of gate-level designs, including propagation delay and setup/hold times.	1	2	2	1	0	1	3	2	L2, L4, L5

SYLLABUS

UNIT–I: Sources of Power Dissipation **12 Hours**

Introduction, Short-Circuit Power Dissipation, Switching Power Dissipation, Dynamic Power for a Complex Gate, Reduced Voltage Swing, Switching Activity, Leakage Power Dissipation, p–n

Junction Reverse-Biased Current, Band-to-Band Tunneling Current, Sub threshold Leakage Current, Short-Channel Effects. **COs–CO1**

UNIT-2: Supply Voltage Scaling for Low Power **12 Hours**

Device Feature Size Scaling, Constant-Field Scaling, Constant-Voltage Scaling, Architectural-Level Approaches: Parallelism for Low Power, Pipelining for Low Power, Combining Parallelism with Pipelining, Voltage Scaling Using High-Level Transformations: Multilevel Voltage Scaling Challenges in MVS Voltage Scaling Interfaces, Static Timing Analysis Dynamic Voltage and Frequency Scaling. **COs–CO2**

UNIT-3: Switched Capacitance Minimization **12 Hours**

Probabilistic Power Analysis: Random logic signals, probability and frequency, probabilistic power analysis techniques, signal entropy, Bus Encoding: Gray Coding, One-Hot Coding, Bus-Inversion, T0 Coding, Clock Gating, Gated-Clock FSMs FSM State Encoding, FSM Partitioning, Pre computation, Glitching Power Minimization. **COs–CO3**

UNIT-4: Leakage Power Minimization **12 Hours**

Fabrication of Multiple Threshold Voltages, Multiple Channel Doping, Multiple Oxide CMOS, Multiple Channel Length, Multiple Body Bias, VTCMOS Approach, MTCMOS Approach, Power Gating, Clock Gating Versus Power Gating, Power-Gating Issues, Isolation Strategy, State Retention Strategy, Power-Gating Controller, Power Management, Combining DVFS and Power Management. **COs–CO4**

UNIT-5: Low power clock distribution & Simulation Power Analysis **12 Hours**

Low power clock distribution: Power dissipation in clock distribution, single driver versus distributed buffers, Zero skew versus tolerable skew, chip and package co design for clock network. Simulation Power Analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, architecture level analysis, data correlation analysis of DSP systems, Monte Carlo Simulation. **COs–CO5**

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Text Books:

1. Low-Power VLSI Circuits and Systems, Ajit Pal, SPRINGER PUBLISHERS
2. Practical Low Power Digital Vlsi Design, Gary Yeap Motorola, Springer Science Business Media, LLC.

Reference Books:

1. Low Power CMOS Design – Anantha Chandrakasan, IEEE Press/Wiley International, 1998.
2. MassoudPedram, Jan M. Rabaey , "Low power design methodologies ", Kluwer Academic Publishers.
3. Low Power CMOS VLSI Circuit Design – A. Bellamour, M. I. Elamasri, Kluwer Academic Press, 1995.

Web References:

1. https://archive.nptel.ac.in/courses/106/105/106105034/
2. https://www.coursera.org/specializations/vlsi-chip-design-with-cps

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)

L1	25	30
L2	35	30
L3	40	20
L4	--	10
L5	--	10
Total (%)	**100**	**100**

Sample Short and Long Answers Questions of Various Cognitive Levels:

L1: Remember

1. What is meant by reduced voltage swing, and why is it used?
2. What is static timing analysis (STA), and how is it used in digital circuit design?
3. What is signal entropy, and how is it used in power analysis?
4. What is the concept of multiple threshold voltages in CMOS fabrication?
5. What is the difference between zero skew and tolerable skew in clock distribution?

L2: Understand

1. Describe how short-circuit power dissipation differs from dynamic and static power dissipation.
2. Explain the principles behind constant-voltage scaling and its impact on power consumption and device speed.
3. Describe how glitching impacts power dissipation and the importance of minimizing glitches.
4. Describe how multiple channel doping affects the electrical characteristics of a semiconductor device.
5. Describe the role of chip and package co-design in optimizing clock distribution.

L3: Apply

1. Given the reverse-bias voltage, calculate the reverse-biased current for a p-n junction diode.
2. Apply knowledge of MVS challenges to propose solutions for improving voltage scaling techniques.
3. Apply One-Hot coding to a digital circuit and estimate its impact on power consumption
4. Apply the concept of multiple channel lengths to a semiconductor design to optimize performance and power efficiency.
5. Apply SPICE simulation to analyze the power consumption of a given circuit design.

L4: Analyzing

1. Analyze the contribution of reverse-biased current to leakage power dissipation in a CMOS circuit.
2. Analyze the impact of DVFS on system performance and power consumption in various operating conditions.
3. Analyze how pre-computation can be used to optimize power consumption in various types of digital circuits.
4. Analyze the advantages and limitations of the VTCMOS approach compared to other power management techniques.
5. Analyze how gate-level simulation results can be used to identify power inefficiencies in a circuit.

L5: Evaluating

1. Evaluate design techniques to mitigate the effects of band-to-band tunneling in advanced semiconductor devices.
2. Design a parallel computing system optimized for low power consumption and explain your design choices.
3. Evaluate the advantages and limitations of bus-inversion encoding in practical digital designs.
4. Evaluate the effectiveness of combining DVFS with power management techniques in different types of digital and analog systems.
5. Evaluate the effectiveness of data correlation analysis in optimizing power consumption for different DSP applications.

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MTVDPC1207 **MIXED SIGNAL IC DESIGN LAB** **0 0 4 2**

Course Objectives:

1. Develop the ability to design both analog and digital circuits with a focus on integrating these components within a single IC.
2. Perform simulations using appropriate software (e.g., SPICE, Cadence, or similar) to analyze the behavior and performance of mixed signal circuits.
3. Learn how to design IC layouts, including placement and routing of analog and digital components.
4. Develop skills in testing and characterizing mixed signal ICs to ensure they meet design specifications.
5. Learn how to integrate analog and digital subsystems within an IC to achieve desired functionality and performance.

At the end of the course, students will be able to:

Course Code	Course Outcomes	Mapping with POs and PSOs								Dok
		PO1	PO2	PO3	PO4	PO5	PO6	PS01	PS02	
MTVDPC1207.1	Extend the concept of phase locked loop for designing PLL application with minimum jitter	3	3	2	0	0	1	3	2	L4,L5
MTVDPC1207.2	Design different A/D/D/A converters for real time applications and Design of VCO	3	2	2	0	1	1	2	2	L3,L4,L5
MTVDPC1207.3	Analyze the stability of compensated op-amp circuits and Optimize design parameters to minimize the influence of parasitics on the circuit's performance.	3	2	2	1	0	1	2	3	L2,L3

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List of Experiments

1. Fully compensated op-amp with resistor and miller compensation **COs: CO2**
2. High speed comparator design
   a. Two stage cross coupled clamped comparator
   b. Strobed Flip-Flop **COs: CO2**
3. Data converter **COs: CO2**
4. Switched capacitor circuits **COs: CO2**
   a. Parasitic sensitive integrator
   b. Parasitic insensitive integrator **COs: CO2**
5. Design of PLL **COs: CO2**
6. Design of VCO **COs: CO2**

7. Bandgap reference circuit **COs: CO2**
8. Layouts of All the circuits Designed and Simulated. **COs: CO2**

Text Books:

1. David A Johns, Ken Martin: Analog IC design, Wiley 2008.
2 R Gregorian and G C Temes: Analog MOS integrated circuits for signal processing, Wiley 1986

Reference Books:

1 Roubik Gregorian: Introduction to CMOS Op-amps and comparators, Wiley, 2008.
2 Behzad Razavi, RF Microelectronics Prentice Hall of India, 2001
3 Thomas H. Lee, The Design of CMOS Radio Integrated Circuits, Cambridge University Press.
4 Roubik Gregorian, Introduction to CMOS OpAmp and Comparators, Wiley, 1999.

Web References:

1. https://ioe.iitm.ac.in/project/rf-analog-and-mixed-signal-integrated-circuits/
2. https://www.sciencedirect.com/topics/engineering/mixed-signal-integrated-circuits

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	30	20
L2	30	40
L3	40	40
Total (%)	**100**	**100**

Lab Experiments of Various Cognitive Levels:

Note: All Experiments to be performed.

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MTVDPC1208 PHYSICAL DESIGN AUTOMATION LAB 0 0 4 2

Course Objectives:

1. Understand basic concepts such as vertices, edges, paths, cycles, and connectivity.
2. Study and implement algorithms for finding the shortest path in weighted graphs
3. Explore current research trends and innovations in the field of group migration.
4. Learn the principles of simulated annealing, including the annealing schedule, acceptance criteria, and its analogy to physical annealing processes.
5. Study algorithms for problems such as Line Intersection Detection and Point-Line Distance Calculation.

At the end of the course, students will be able to:

Course Code	Course Outcomes	Mapping with POs and PSOs								Dok
		PO1	PO2	PO3	PO4	PO5	PO6	PS01	PS02	
MTVDPC1208.1	Implement and analyze Depth-First Search (DFS) and Breadth-First Search (BFS) algorithms.	3	3	3	0	1	1	2	2	L4,L5
MTVDPC1208.2	Understand applications in graphics, CAD systems, and spatial analysis, Understand the differences between static and dynamic routing, unicast and multicast routing, and intra-domain vs. inter-domain routing.	2	3	3	0	1	0	2	3	L2,L4,L5
MTVDPC1208.3	Gain hands-on experience by coding graph algorithms in programming languages such as Python, C++, or Java, Differentiate between various types of floor plans, such as those used in VLSI design, architectural layouts, and product packaging.	2	1	3	1	0	1	2	3	L2,L5

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List of Experiments

1 **Graph algorithms**
Graph search algorithms COs: CO2

	i) Depth first search ii) Breadth first search	
2	Spanning tree algorithm i) Kruskal"s algorithm	COs: CO2
3	Shortest path algorithm i) Dijkstra algorithm ii) Floyd- Warshall algorithm	COs: CO2
4	Steiner tree algorithm	COs: CO2
	Computational geometry algorithm	
5	i) Line sweep method ii) Extended line sweep method	COs: CO2
	Partitioning algorithms	
6	Group migration algorithms a) Kernighan –Lin algorithm	COs: CO2
7	Group migration algorithms b) Extensions of Kernighan-Lin algorithm i) Fiduccias –Mattheyses algorithm ii) Goldberg and Burstein algorithm	COs: CO2
8	Simulated annealing and evolution algorithms i) Simulated annealing algorithm ii) Simulated evolution algorithm	COs: CO2
9	Metric allocation method	COs: CO2
	Floor planning algorithms	
10	i) Constraint based methods ii) Integer programming-based methods iii) Rectangular dualization based methods iv) Hierarchical tree-based methods v) Simulated evolution algorithms vi) Time driven Floor planning algorithms	COs: CO2
11	**Routing algorithms**	
12	I) Two terminal algorithms a) Maze routing algorithms i)Lee"s algorithm ii) Soukup"s algorithm iii) Hadlock algorithm b) Line-Probe algorithm c) shortest path-based algorithm II) Multi terminal algorithm a) Steiner tree-based algorithm i) SMST algorithm ii) Z-RST algorithm	COs: CO2 COs: CO2

Text Books:

1. NaveedShervani, Algorithms for VLSI Physical Design Automation, 3rd Edition, Kluwer Academic, 1999.
2. Charles J Alpert, Dinesh P Mehta, Sachin S Sapatnekar, Handbook of Algorithms forPhysical Design Automation, CRC Press, 2008

Web References:

1. https://nptel.ac.in/courses/117106092
2. https://onlinecourses.nptel.ac.in/noc24_cs70/preview
3. https://en.wikipedia.org/wiki/Very-large-scale_integration

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	30	20
L2	30	40
L3	40	40
Total (%)	**100**	**100**

Note: Minimum 10 Experiments to be performed.

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MTVDPE21051 NANO MATERIALS AND NANO TECHNOLOGY 3 0 0 3

(VLSI Design)

Course Objectives:

1. To introduce the fundamentals of nano materials and nanotechnologies, highlighting their unique features, synthesis methods, size-dependent properties, and diverse applications.
2. To provide foundational knowledge on the classification, synthesis, properties, and applications of low-dimensional nano materials, with a focus on carbon-based nanostructures.
3. To provide an overview of micro- and nanolithography techniques, MEMS fabrication technologies, and emerging applications including nano phononics.
4. To impart knowledge on the synthesis, properties, growth mechanisms, and applications of carbon nano tubes (CNTs), including both single- and multi-walled structures.
5. To explore the properties and applications of ferroelectric materials, molecular and nanoelectronics, and nano-enabled solutions in biological, environmental, membrane, and polymer-based technologies.

Course Outcomes:

At the end of the course, students will be able to:

Course Code	Course Outcomes	Mapping with POs and PSOs							Do K
		PO1	PO2	PO3	PO4	PO5	PSO1	PSO2	
MTVDPE 21051.1	Understand the fundamental science behind the design and fabrication of nano scale systems.	3	2	-	-	-	3	-	L1, L2
MTVDPE 21051.2	Develop the ability to formulate innovative engineering solutions for current challenges and emerging technologies.	-	3	3	-	-	-	3	L3
MTVDPE 21051.3	Gain interdisciplinary competence to conceptualize and execute projects across diverse application domains.	-	-	3	-	-	-	2	L3, L4
MTVDPE 21051.4	Acquire in-depth knowledge of fabrication and characterization techniques for nano scale materials and devices.	-	2	3	3	3	2	3	L4
MTVDPE 21051.5	Bridge the gap between theoretical concepts and practical implementation by defining system development boundaries.	-	-	3	3	3	3	2	L4, L5

SYLLABUS

UNIT –I **16 Hours**

Introduction of nano materials and nanotechnologies, Features of nanostructures, Applications of nano materials and technologies. Nano dimensional Materials 0D, 1D, 2D structures, Size Effects, Fraction of Surface Atoms. Specific Surface Energy and Surface Stress, Effect on the Lattice Parameter, Phonon Density of States, the General Methods available for the Synthesis of Nano structures, precipitate reactive– hydrothermal/solvo thermal methods, suitability of such methods for scaling **CO's–CO1**

Self Learning Topics: Potential uses of thermal methods

UNIT -II: **12 Hours**

Fundamentals of nano materials, Classification, Zero-dimensional nanomaterials, One-dimensional

Nanomaterials, Two-dimensional nanomaterials, Three dimensional nanomaterials. Low-Dimensional Nano materials and its Applications, Synthesis, Properties, and **CO's–CO2**

Self Learning Topics: Applications of Low Dimensional Carbon-Related Nano materials

UNIT -III: **14 Hours**

Micro and Nanolithography Techniques, Emerging Applications Introduction to Micro electromechanical Systems (MEMS), Advantages and Challenges of MEMS, Fabrication Technologies, Surface Micromachining. Nano Phonics. **CO's–CO3**

Self Learning Topics: Bulk Micromachining, Molding.

UNIT -IV: **16 Hours**

Introduction, Synthesis of CNT: Arc-discharge, Laser-ablation, Catalytic growth, Growth mechanisms of CNT"s: Multi-walled nano tubes, Single-walled nano tubes Optical properties of CNT"s, Electrical transport in perfect nano tubes, Applications as case studies. **CO's–CO4**

Self Learning Topics: Synthesis and Applications of CNT's.

UNIT -V: **12 Hours**

Ferroelectric materials, coating, molecular electronics and nano electronics, biological and environmental, membrane based application, polymer based application. **CO's–CO5**

Self Learning Topics: Properties Ferroelectric materials

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Approved in ACM No: 02

Text Books:

1. Kenneth J. Klabunde and Ryan M. Richards, "Nanoscale Materials in Chemistry", 2nd edition, John Wiley and Sons, 2009.
2. I Gusev and A ARempel, "Nanocrystalline Materials", Cambridge International Science Publishing, 1st Indian edition by Viva Books Pvt. Ltd. 2008.
3. B. S. Murty, P. Shankar, Baldev Raj, B. B. Rath, James Murray, "Nanoscience and Nanotechnology", Tata McGraw Hill Education 2012.

Reference Books:

1. Bharat Bhushan, "Springer Handbook of Nanotechnology", Springer, 3rd edition, 2010.
2. Kamal K. Kar, "Carbon Nanotubes: Synthesis, Characterization and Applications", Research Publishing Services; 1 st edition.

Web References:

1. https://www.edx.org/learn/electronics/purdue-university-fundamentals-of-nanomaterials-and-nanotechnology.
2. https://nptel.ac.in/courses/118102003

Internal Assessment Pattern

Cognitive Level	Internal Assessment # 1 (%)	Internal Assessment # 2 (%)
L1	30	--
L2	30	--
L3	40	30
L4	--	40
L5	--	30
Total (%)	**100**	**100**

Short and Long Answers Questions of Various Cognitive Levels:

L1: Remember

1. Define nano materials and nanotechnologies with examples.
2. State the significance of surface stress in nano scale systems.
3. Define low-dimensional nano materials with appropriate examples.
4. List the different fabrication techniques used in MEMS.
5. List three major synthesis techniques for CNTs.
6. What are the essential characteristics of nano electronic devices?

L2: Understand

1. Discuss the influence of dimensionality (0D, 1D, 2D) on electronic and optical properties.
2. Explain how dimensionality affects the electronic properties of nano materials.
3. Explain the principle of photolithography in the context of micro fabrication.
4. Discuss how CNTs exhibit unique optical properties.
5. Explain the working principle of ferroelectric memory.

L3: Apply

1. Determine a suitable synthesis method for a given nanostructure and justify your choice based on scalability and Cost.
2. Apply the concept of quantum confinement to describe the behavior of electrons in 0D materials.
3. Apply knowledge of MEMS fabrication techniques to design a pressure sensor.
4. Apply the laser ablation method to design a lab-scale setup for CNT synthesis.
5. Demonstrate how polymer-based nanocarriers can be used in drug delivery.

L4: Analyzing

1. Analyze the impact of dimensionality on the mechanical properties of carbon nano materials.
2. Examine the influence of synthesis conditions on the purity and structure of carbon nanotubes.
3. Compare and contrast photolithography and electron beam lithography in terms of resolution and throughput.
4. Analyze the advantages and disadvantages of arc-discharge vs catalytic growth in terms of scalability and purity.
5. Analyze the impact of size reduction on the ferroelectric properties of thin films.

L5: Evaluating

1. Assess the environmental and health risks associated with the use of carbon nano materials.
2. Justify the use of graphene over carbon nanotubes in flexible electronics based on their properties.
3. Evaluate the feasibility of integrating MEMS devices into flexible electronics.
4. Critically evaluate the limitations of laser ablation in commercial CNT production.
5. Assess the environmental implications of using nano-coatings in marine industries.

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MTVDPE21052 **Digital System Design and Verification** **3 0 0 3**
(VLSI Design)

Course Objectives:

1. Understand foundational concepts of digital systems including combinational and sequential circuits, FSMs, and key hardware modules like ALUs, FIFOs, and multipliers.
2. Develop proficiency in HDL design using Verilog/VHDL, including simulation, testbench creation, and integration of IPs for prototyping and performance evaluation.
3. Apply verification techniques using System Verilog, including assertions, object-oriented test benches, randomization, and fault testing methods such as BIST and JTAG.
4. Analyze physical design challenges, including signal integrity, timing delays, power issues, and the effects of process technologies on chip performance and reliability.
5. Explore programmable logic devices and architectures, including PALs, FPGAs, and ASIC flows, along with their evolution, programming methods, and application in reconfigurable systems.

Course Outcomes:

At the end of the course, students will be able to:

Course Code	Course Outcomes	Mapping with POs and PSOs							DoK
		PO1	PO2	PO3	PO4	PO5	PSO1	PSO2	
MTVDPE21052.1	Demonstrate familiarity with front-end digital design principles and verification techniques.	3	-	-	-	-	3	2	L1, L2
MTVDPE21052.2	Design and implement reusable test environments to streamline the verification process.	3	2	2	-	2	2	3	L2, L3
MTVDPE21052.3	Apply verification methodologies to efficiently and effectively verify complex digital designs.	3	3	2	-	-	2	3	L3
MTVDPE21052.4	Utilize industry-standard EDA tools such as Cadence and Mentor Graphics for simulation and debugging.	3	-	2	2	3	3	2	L6
MTVDPE21052.5	Develop skills to analyze and improve the performance, scalability, and accuracy of verification processes.	3	2	3	2	-	2	2	L4, L5

SYLLABUS

UNIT –I **14 Hours**

Revision of basic Digital systems: Combinational Circuits, Sequential Circuits, Logic families. Synchronous FSM and asynchronous design, Meta-stability, Clock distribution and issues, basic building blocks like PWM module, pre-fetch unit, programmable counter, FIFO, Booth's multiplier, ALU, Barrel shifter. **CO's–CO1**

Self learning topics: Comparison between different logic families

UNIT -II: **12 Hours**

Verilog/VHDL Comparisons and Guidelines, Verilog: HDL fundamentals, simulation, and Test bench design, Examples of Verilog codes for combinational and sequential logic, Verilog AMS.IP and Prototyping: IP in various forms: RTL Source code, Encrypted Source code, Soft IP, Netlist, Physical IP, Speed issues. **COs–CO2**

Self learning topics: Use of external hard IP during prototyping,

UNIT -III: **12 Hours**

System Verilog and Verification: Verification guidelines, Data types, procedural statements and routines, connecting the test bench and design, Assertions, Basic OOP concepts, Randomization. Testing of logic circuits: Fault models, BIST, JTAG interface **COs–CO3**

Self learning topics: Introduction to basic scripting language: Perl, Tcl/Tk

UNIT -IV: **15 Hours**

Current challenges in physical design: Roots of challenges, Delays: Wire load models Generic PD flow, Challenges in PD flow at different steps, SI Challenge - Noise & Crosstalk, IR Drop, Process effects: Process Antenna Effect &Electro migration. **COs–CO4**

Self learning topics: Flow chart for Physical Design

UNIT -V: **15 Hours**

Programmable Logic Devices: Introduction, Evolution: PROM, PLA, PAL, Architecture of PAL's, Applications, Programming PLD's, FPGA with technology: Anti-fuse, SRAM, EPROM, MUX, FPGA structures, and ASIC Design Flows, Programmable Interconnections. **COs–CO5**

Self learning topics: Course grained reconfigurable device.

Board of Studies : Electronics and Communication Engineering
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Approved in ACM No: 02

Text Books:

1. Douglas Smith, “HDL Chip Design: A Practical Guide for Designing, Synthesizing &
2. Simulating ASICs & FPGAs Using VHDL or Verilog”, Doone publications, 1998
3. Samir Palnitkar, “Verilog HDL: A guide to Digital Design and Synthesis”, Prentice Hall, 2nd Edition, 2003

Reference Books:

1. Doug Amos, Austin Lesea, Rene Richter, “FPGA based Prototyping Methodology Manual”, Synopsys Press, 2011.
2. Christophe Bobda, “Introduction to Reconfigurable Computing, Architectures, Algorithms and Applications”, Springer, 2007.
3. Janick Bergeron, “Writing Test benches: Functional Verification of HDL Models”, 2nd Edition, Springer, 2003.

Web References:

1. https://www.cadence.com/en_US/home/training/all-courses/86366.html.
2. https://onlinecourses.nptel.ac.in/noc24_ee17/preview.
3. https://www.coursera.org/learn/digital-systems.

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	30	--
L2	40	--
L3	30	20
L4	--	30
L5	--	30
L6		20

Total (%)	100	100

Short and Long Answers Questions of Various Cognitive Levels:

L1: Remember

1. Define metastability and explain its impact in digital systems.
2. List the basic data types used in Verilog HDL.
3. Define assertion in System Verilog and give an example.
4. List the factors that contribute to IR drop in integrated circuits.
5. List the different types of programmable logic devices and their primary applications.

L2: Understand

1. Explain the operation of a programmable counter with an appropriate timing diagram.
2. Differentiate between Verilog and VHDL in terms of syntax and simulation behavior.
3. Explain the role of a test bench in Verilog simulation with an example.
4. Explain the difference between initial and always blocks in System Verilog.
5. Describe the significance of process antenna effect in physical design.

L3: Apply

1. Simulate a synchronous FSM for a traffic light controller and verify its behavior using a testbench
2. Simulate a sequential circuit (e.g., D flip-flop with reset) using Verilog and validate its waveform.
3. Write a System Verilog module to connect a testbench to a design using interfaces.
4. Design a layout strategy that minimizes IR drop in a system-on-chip (SoC) design.
5. Develop a VHDL design for an FPGA that implements a counter with reset and enable inputs.

L4: Analyzing

1. Compare Booth's multiplication algorithm with traditional binary multiplication for speed and area.
2. Identify and explain the key differences in simulation behavior when using blocking vs. non-blocking assignments in Verilog.
3. Break down the flow of a JTAG interface and identify its role in boundary scan testing.
4. Analyze the trade-offs between optimizing for delay and minimizing crosstalk in high-speed PCB design.
5. Break down the steps in an ASIC design flow and evaluate the challenges at each stage.

L5: Evaluating

1. Evaluate different logic families (CMOS, TTL, ECL) based on speed, power, and noise immunity for designing high-performance systems.
2. Evaluate different types of assertions (immediate vs concurrent) for use in pipelined design verification.
3. Assess the challenges and solutions related to process antenna effects in the context of multi-layer metalization in advanced nodes.

L6: Creating

1. Analyze the impact of wire load models on the performance of a digital system and propose a solution to mitigate the effects.

2. Design a power grid for a complex digital system that minimizes IR drop and ensures reliable operation.

3. Develop a methodology to optimize the physical design of a digital system for reduced crosstalk and noise.

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MTVDPE21053 **PHOTONICS** **3 0 0 3**
(VLSI Design)

Course Objectives:

1. To understand the structure, working principles, and applications of various laser systems and optical amplifiers.
2. To study the key properties of laser radiation such as line width, coherence, divergence, and methods of pulse modulation like Q-switching and mode-locking.
3. To understand the functioning of opto-electronic devices, including P-N junctions, carrier recombination, quantum wells, and the principles behind LED efficiency.
4. To explore the structures and performance of advanced opto-electronic devices like quantum well lasers, photodiodes, APDs, and laser diodes.
5. To study the different modulation techniques of light using electro-optic, acousto-optic, and magneto-optic effects for applications like switching and signal processing.

Course Outcomes:

At the end of the course, students will be able to:

Course Code	Course Outcomes	Mapping with POs and PSOs								Do K
		PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	
MTVDPE21053.1	Classify the Optical sources and detectors and to discuss their principle.	3	2	1	1	2	0	3	1	L1, L2
MTVDPE21053.2	Familiar with Design considerations of fiber optic systems.	3	3	3	2	2	2	3	1	L3
MTVDPE21053.3	Design and conduct experiments on optical fibers, sources, detectors, and analyze results to draw valid conclusions..	2	3	2	3	3	2	2	3	L3
MTVDPE21053.4	Apply atomic physics principles to design optical fibers and photonic crystals, calculating material properties.	3	2	3	2	1	0	3	2	L3, L4
MTVDPE21053.5	Apply physics tools, methodologies, and conventions to test, communicate, and integrate course concepts in new situations.	2	3	2	3	3	2	2	3	L5, L6

SYLLABUS

UNIT –I: Laser systems **14 Hours**

General description, Laser structure, Single mode laser theory, Excitation mechanism and working of: CO2, Nitrogen, Argon ion, Excimer, X-ray, Free-electron, Dye, Nd:YAG,Alexanderite and Ti:sapphire lasers, Diode pumped solid state laser, Optical parametric oscillator (OPO) lasers. Optical amplifiers- Semiconductor optical amplifiers, Erbium doped waveguide optical amplifiers, Raman amplifiers, Fiber Lasers. **CO's–CO1**

Self Learning Topics: Laser Applications-Lasers in Isotope separation, Laser interferometry and speckle metrology, Velocity measurements.

UNIT -II: Properties of laser Radiation **14 Hours**

Introduction, Laser line width, Laser frequency stabilization, Beam divergence, Beam coherence, Brightness, Focusing properties of laser radiation, Q-switching, Methods of Q- switching:Rotating-

mirror method, Electro-optic Q-switching, Acoustic-optic Q-switching and Passive Q-switching, Mode locking, Methods of mode locking: Active and passive mode locking techniques, **CO's–CO2**

Self Learning Topics: Frequency doubling and Phase conjugation.

UNIT -III: Opto-electronic Devices-I **14 Hours**

Introduction, P-N junction diode, Carrier recombination and diffusion in P-N junction, Injection efficiency, Internal quantum efficiency, Hetero-junction, Double hetero-junction, Quantum well, Quantum dot and Super lattices; LED materials, Device configuration and efficiency. **CO's–CO3**

Self Learning Topics: Characteristics of semiconductor diodes.

UNIT -IV: Opto-electronic Devices -II **14 Hours**

Light extraction from LEDs, LED structures-single hetero structures, double hetero structures, Device performances and applications, Quantum well lasers; Photo diode and Avalanche photodiodes(APDs), Laser Diodes-Amplification, Feedback and oscillation, Power and efficiency. Spectral and spatial characteristics. **CO's–CO4**

Self Learning Topics: Spectral and spatial characteristics of LASER diode.

UNIT -V: Modulation of Light **14 Hours**

Introduction, Birefringence, Electro-optic effect, Pockels and Kerr effects, Electro-Optic Phase modulation, Electro-optic amplitude modulation, Electro-optic modulators: scanning and switching, Acousto-optic effect, Acousto-optic modulation, Raman Nath and Bragg modulators: deflectors and spectrum analyzer, Magneto-optic effect, Faraday rotator as an optical isolator. **CO's–CO5**

Self Learning Topics: Advantages of optical modulation.

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Text Books:

1. Lasers: Principles and applications by J.Wilson and J.F.B.Hawkes, Prentice, Hall of India, New Delhi, 1996.
2. Laser fundamentals, W.T.Silfvast, Foundation books, New Delhi, 1999.
3. Semi conductoropto electronics devices, P. Bhattacharya, Prentice – Hall of India,New Delhi, 1995.17

Reference Books:

1. Optical fiber communications, John M. Senior, Prentice-Hall of India, New Delhi, 2001
2. Optoelectronics: An Introduction, J.WilsonAndJ.F.B.Hawkes, Prentice-Hall of India, New Delhi, 1996.
3. Electro-Optical devices, M.A. Karim, Boston, Pws-Kent Publishers, 1990.

Web References:

1. https://onlinecourses.nptel.ac.in/noc21_ee87/preview
2. https://www.mooc-course.com/course/nanophotonics-and-detectors-coursera/
3. https://onlinecourses.nptel.ac.in/noc21_ee98/preview

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	30	--
L2	30	--
L3	40	20
L4	--	30
L5	--	30
L6	--	20
Total (%)	**100**	**100**

Short and Long Answers Questions of Various Cognitive Levels:

L1: Remember

1. Define the basic structure of a laser system.
2. What are the main characteristics of laser beam coherence?
3. Define carrier recombination in a P-N junction diode.
4. What is the structural difference between a single and a double heterostructure LED?
5. What is the principle of operation of a Faraday rotator?

L2: Understand

1. Explain the principle of operation of a CO_2 laser and how it differs from a nitrogen laser.
2. Explain the concept of laser frequency stabilization and its importance in high-precision applications.
3. Explain the process of carrier diffusion in a forward-biased P-N junction.
4. Discuss the factors that affect light extraction efficiency in LED devices.
5. Discuss the importance of modulation bandwidth in high-speed optical communication.

L3: Apply

1. Apply the principle of Raman amplification to improve the performance of an optical communication system.
2. How would you design a laser system that uses mode locking to produce femtosecond pulses? What factors would you consider in your design?
3. Apply the concept of carrier recombination to predict how LED output changes with temperature.
4. Apply the concept of double hetero structures to design a high-efficiency LED for optical communication.
5. How would you use a Faraday rotator to design an optical isolator in a laser system?

L4: Analyzing

1. Analyze the differences between a semiconductor optical amplifier and a fiber laser in terms of their applications and efficiency.

2. Compare and contrast the rotating-mirror method and electro-optic Q-switching in terms of their effectiveness, efficiency, and application areas.
3. Analyze how material choice affects the efficiency and emission wavelength of an LED.
4. Distinguish between the amplification mechanisms in photodiodes versus laser diodes.
5. How does birefringence influence the efficiency of modulation in various materials?

L5: Evaluating

1. Assess the potential challenges in scaling up a free-electron laser for industrial use, especially in terms of Cost and efficiency.
2. Evaluate the potential impact of laser line width on the performance of a precision laser-based measurement system. How would you minimize the line width in such a system?
3. Justify the use of double hetero structures in LEDs for high-temperature environments.
4. Critically evaluate different LED structure designs for maximizing external quantum efficiency.

L6: Creating

1. Design an electro-optic phase modulator that can modulate the phase of a laser beam at a frequency of 10 GHz.
2. Develop an electro-optic amplitude modulator that can modulate the amplitude of a laser beam with a modulation depth of 90%.
3. Create a system that uses electro-optic modulators for scanning and switching applications in a laser-based material processing system.

Chairperson
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MTVDOE2101 FUNDAMENTALS OF NANO TECHNOLOGY 3 0 0 3

(Open Elective –I)

Course Objectives:

1. Define nanotechnology, its history, and its significance in various fields.
2. Understand various methods for synthesizing and fabricating nano materials, including top-down and bottom-up approaches.
3. Study the unique properties of nano materials, including structural, thermal, chemical, magnetic, optical, and electronic properties.
4. Discuss various applications of nanotechnology in fields such as electronics, medicine, energy, and materials science.
5. Learn various techniques for characterizing nano materials, including microscopy, spectroscopy, and diffraction methods.

Course Outcomes:

At the end of the course, students will be able to:

Course Code	Course Outcomes	Mapping with POs and PSOs					DoK
		PO1	PO2	PO3	PO4	PO5	
MTVDOE2101.1	Explain its fundamental principles, including the unique properties of nano materials.	3	2	-	-	-	L1, L2
MTVDOE2101.2	Design and synthesize nano materials using various techniques, including top-down and bottom-up approaches.	-	3	3	-	-	L3
MTVDOE2101.3	Analyze and characterize nano materials using various techniques, including microscopy, spectroscopy, and diffraction methods.	-	-	3	-	-	L3, L4
MTVDOE2101.4	Apply nanotechnology to solve real-world problems in fields such as electronics, medicine, energy, and materials science.	-	2	3	3	3	L3
MTVDOE2101.5	Evaluate the potential impact of nanotechnology on society, including its benefits and risks, and discuss its future directions.	-	-	3	3	3	L4, L5

Syllabus

UNIT- I **12 Hours**

Over View of Nanotechnology: Definition, historical development, properties, design and fabrication Nano systems, working principle, applications and advantages of nano system. Nano materials: ordered oxides, Nano arrays. **CO's-CO1**

Self Learning Topics: Potential health effects with nano materials.

UNIT –II **12 Hours**

Nano defects, Nano Partiles and Nano layers: Nano defects in crystals, applications, Nuclear Track nano defects. Fabrication of nano particles, LASER ablation, sol gels precipitation of quantum dots. Nano layers PVD, CVD, Epitaxy and ion implantation, formation of Silicon oxide, chemical composition. **CO's-CO2**

Self Learning Topics: Doping properties, optical properties.

UNIT- III **16 Hours**

Nano structuring: Nano photolithography, Introduction, techniques-optical-electron beam ion beam- X-ray and Synchrotron, nanolithography for microelectronic industry, nano polishing of Diamond, Etching of Nano structures , Nano imprinting technology – Focused ion beams - LASER interference Lithography nano arrays. **CO's-CO3**

Self Learning Topics: Near-Field Optics

UNIT- IV **16 Hours**

Science and Synthesis of Nano Materials: Classification of nano structures, Effects of nano scale dimensions on various properties: structural, thermal, chemical, magnetic, optical and electronic properties fluid dynamics, Effect of nano scale dimensions on mechanical properties - vibration, bending, fracture Nanoparticles, Sol-Gel Synthesis, Inert Gas Condensation, High energy Ball Milling, Plasma Synthesis, Electro deposition and other techniques. Synthesis of Carbon nanotubes Solid carbon source-based production techniques, Gaseous carbon source-based production techniques, Diamond like carbon coating. **CO's-CO4**

Self Learning Topics: Top down and bottom up processes.

UNIT –V **14 Hours**

Characterization of Nano Materials: Nano-processing systems, Nano measuring systems, characterization, analytical imaging techniques: microscopy techniques, electron microscopy scanning electron microscopy, confocal LASER scanning microscopy, transmission electron microscopy, transmission electron microscopy, scanning tunnelling microscopy, atomic force microscopy, diffraction techniques, spectroscopy techniques. **CO's-CO5**

Self Learning Topics: Raman spectroscopy, 3D surface

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Approved in BOS No: 02, 30th May,2025

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Text Books:

1. Tai-Ran Hsu, MEMS and Microsystems Design and Manufacture, Tata-McGraw Hill, 2002.
2. Fahrner W.R., Nanotechnology and Nano electronics, Springer (India) Private Ltd., 2011.
3. Mark Madou, Fundamentals of Micro fabrication, CRC Press, New York, 1997.
4. Norio Taniguchi, Nano Technology, Oxford University Press, New York, 2003.

Reference Books:

1. Mohamed Gad-el-Hak, MEMS Handbook, CRC press, 2006.
2. Waqar Ahmed and Mark J. Jackson, Emerging Nanotechnologies for Manufacturing,

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1 (%)	Internal Assessment #2 (%)

L1	30	--
L2	30	--
L3	40	40
L4	--	30
L5	--	30
Total (%)	**100**	**100**

L1: Remembering

1. What is the definition of nanotechnology?
2. Name three techniques used for synthesizing nanoparticles.
3. What is the difference between top-down and bottom-up approaches in nanotechnology?

L2: Understanding

1. Explain the unique properties of nano materials and how they differ from bulk materials.
2. Describe the principle of Atomic Force Microscopy (AFM) and its applications in nanotechnology.
3. How do the properties of nanoparticles change with their size and shape?

L3: Applying

1. Design a simple experiment to synthesize silver nanoparticles using a chemical reduction method.
2. Calculate the surface area-to-volume ratio of a nanoparticle with a given diameter.
3. Propose a potential application of carbon nanotubes in the field of energy storage.

L4: Analyzing

1. Compare and contrast the properties of nanoparticles synthesized using different methods (e.g., sol-gel vs. laser ablation).
2. Analyze the advantages and limitations of using Scanning Electron Microscopy (SEM) vs. Transmission Electron Microscopy (TEM) for imaging nanoparticles.
3. Discuss the potential environmental impacts of nanoparticles and how they can be mitigated.

L5: Evaluating

1. Evaluate the potential benefits and risks of using nanoparticles in consumer products.
2. Critique the current state of nanotechnology research in a specific field and propose future directions.
3. Assess the effectiveness of different characterization techniques (e.g., AFM, SEM, TEM) for analyzing nanoparticles.

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MTVDOE2102 **Hardware Software Co-Design** **3 0 0 3**

(Open Elective –I)

Course Objectives:

- Define hardware/software co-design, its importance, and its applications.
- Understand data flow modelling, implementation in software and hardware, and analysis of control flow and data flow.
- Learn to design finite state machines with data path (FSMD), micro programmed architectures, and general-purpose embedded cores.
- Study principles of hardware/software communication, synchronization schemes, and on-chip buses.
- Analyze and design hardware/software systems using case studies and practical examples

Course Outcomes:

At the end of the course, students will be able to:

Course Code	Course Outcomes	Mapping with POs and PSOs					DoK
		PO1	PO2	PO3	PO4	PO5	
MTVDOE2102.1	Design and implement hardware/software systems using data flow modelling and implementation techniques.	2	2	-	-	2	L1,L2
MTVDOE2102.2	Analyze and optimize system performance using concurrency and parallelism techniques.	-	2	3	-	-	L2, L3
MTVDOE2102.3	Develop custom architectures, including FSMD and micro programmed architectures.	-	-	3	-	-	L3,
MTVDOE2102.4	Interface hardware and software components, including on-chip buses and coprocessor interfaces.	-	2	3	3	3	L4,L6
MTVDOE2102.5	Apply hardware/software co-design principles to complex systems, including cryptographic coprocessors and digital signal processing systems.	-	-	2	2	2	L4,L5

SYLLABUS

UNIT I: NATURE OF HARDWARE AND SOFTWARE 16 Hours

Hardware, Software, Definition of Hardware/Software Co-Design, Driving factors Platform design space, Application mapping – Dualism of Hardware design and software design, Concurrency and parallelism, Data flow modelling and Transformation. Data Flow Graph, Tokens, actors and queues, Firing rates, firing rules and Schedules, Synchronous data flow graph. **CO's-CO1**

Self learning topics: Control flow modelling, Adding time and resources.

UNIT II: DATA FLOW IMPLEMENTATION 12 Hours

Software Implementation of Data Flow, Converting queues and actors into software, Dynamic Scheduler, Hardware Implementation of Data Flow – single rate SDF graphs into hardware,

Pipelining, Analysis of control flow and data flow – construction of control and data flow graph, Translating C into hardware. **CO's-CO2**

Self learning topics: Designing data path and controller.

UNIT III: DESIGN SPACE OF CUSTOM ARCHITECTURES **15 Hours**

Finite state machines with data path, FSMD design example, Limitations, Micro programmed Architecture, Micro programmed control, microinstruction encoding, Micro programmed data path, micro programmed machine. General purpose Embedded Core, RISC pipeline, Program organization, **CO's-CO3**

Self learning topics: SoC interfaces for custom hardware.

UNIT IV: HARDWARE/ SOFTWARE INTERFACES **17 Hours**

Principles of Hardware/software communication – synchronization schemes, communication constrained versus Computation constrained, Tight and Loose coupling, On-chip buses, Memory mapped interfaces, coprocessor interfaces, custom instruction interfaces, and Coprocessor hardware interface. **CO's-CO4**

Self learning topics: Data and control design, programmer's model.

UNIT V: **14 Hours**

Trivium Cripto coprocessor, Trivium stream cipher algorithm, Trivium for 8- bit platforms, AES coprocessor, CORDIC coprocessor, algorithm and implementation. **CO's-CO1**

Self learning topics: Micro Processor and micro controller architectures.

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TEXT BOOKS:

1. Ralf Niemann, "Hardware/Software Co-Design for Data Flow Dominated Embedded Systems", Kluwer Academic Pub, 1998.
2. Jorgen Staunstrup, Wayne Wolf, "Hardware/Software Co-Design: Principles and Practice", Kluwer Academic Pub, 1997.

REFERENCE BOOKS:

1. Giovanni De Micheli, Rolf Ernst Morgon, Reading in Hardware/Software Co-Design, Kaufmann Publishers, 2001.
2. Patrick Schaumont, A Practical Introduction to Hardware/Software Codesign, 2nd Edition, Springer, 2010.

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	30	--

L2	40	--
L3	30	20
L4	--	30
L5	--	30
L6	--	20
Total (%)	**100**	**100**

L1: Remembering

1. Define hardware/software co-design.
2. What is data flow modelling?
3. Describe finite state machines with data path (FSMD).
4. What is micro programmed architecture?

L2: Understanding

1. Explain the difference between hardware and software design.
2. Describe the role of concurrency and parallelism in hardware/software systems.
3. How do tokens, actors, and queues work in data flow graphs?
4. What is the impact of pipelining on system performance?

L3: Applying

1. Design a simple data flow graph for a given system.
2. Implement a micro programmed architecture for a specific application.
3. Use data flow modeling to optimize a system's performance.
4. Translate a C program into hardware using data flow implementation.

L4: Analyzing

1. Analyze the trade-offs between hardware and software design.
2. Evaluate the impact of concurrency on system performance.
3. Compare and contrast different data flow modelling techniques.
4. Analyze the limitations of custom architectures.

L5: Evaluating

1. Evaluate the effectiveness of data flow modelling in hardware/software co-design.
2. Compare and contrast different hardware/software co-design approaches.
3. Assess the impact of concurrency on system reliability.
4. Evaluate the trade-offs between hardware and software implementation.

L6: Creating

1. Design an on-chip bus architecture for a system-on-chip (SoC) that includes multiple processors, memories, and peripherals.
2. Develop a memory-mapped interface for a hardware accelerator that allows a processor to access its registers and memory spaces.
3. Create a coprocessor interface that enables a processor to offload specific tasks to a hardware accelerator, such as encryption or compression.

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MTVDOE2103 DIGITAL CMOS VLSI DESIGN 3 0 0 3

(Open Elective-I)

Course Objectives:

- Understand MOSFET characteristics, CMOS inverter behavior, and performance parameters.
- Learn static and dynamic CMOS logic design, including pass-transistor and ratioed logic.
- Analyze static and dynamic latches, registers, and timing metrics for sequential circuits.
- Design data path circuits and understand the trade-offs in adders, multipliers, and memory subsystems.
- Gain skills in Verilog HDL for modeling digital systems and high-level synthesis techniques.

Course Outcomes:

At the end of the course, students will be able to:

Course Code	Course Outcomes	Mapping with POs and PSOs						DoK
		PO1	PO2	PO3	PO4	PO5	PO6	
MTVDOE2103.1	Understand MOSFET and CMOS inverter characteristics.	3	3	-	2	-	-	L1, L2
MTVDOE2103.2	Design Combinational Logic Circuits using static and dynamic CMOS logic circuits	-	3	3	2	2	-	L3
MTVDOE2103.3	Analyze timing, latches and registers in sequential circuits**.**	-	3	-	2	2	-	L2, L3
MTVDOE2103.4	Design Arithmetic Units and Memory. Design data path circuits and evaluate memory architectures.	-	3	3	-	2	-	L3,L5
MTVDOE2103.5	Model Digital Systems with Verilog HDL – Use Verilog HDL for digital system modeling and synthesis.	3	3	-	-	3	-	L4,L5

SYLLABUS

UNIT –I MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER 14 Hours

MOSFET Transistor Characteristic under Static and Dynamic Conditions, MOS Transistor Secondary Effects, CMOS Inverter - Static Characteristic, Dynamic Characteristic, Power, Energy, Energy Delay parameters. **CO's–CO1**

Self Learning Topics: Enhancement and depletion mode MOS transistors.

UNIT -II: COMBINATIONAL LOGIC CIRCUITS 14 Hours

Static CMOS Design, Complementary CMOS, Ratioed Logic, Pass-Transistor Logic. Dynamic CMOS Design, Dynamic Logic: Basic Principles, Speed and Power Dissipation of Dynamic Logic, Issues in Dynamic Design, Cascading Dynamic Gates. **COs–CO2**

Self Learning Topics: Logic levels for different logic families.

UNIT -III: SEQUENTIAL LOGIC CIRCUITS 14 Hours

Timing metrics for sequential circuits, Static Latches and Registers, Dynamic Latches and Registers, Pipelines, Pulse and sense amplifier based Registers, Non - Bistable Sequential Circuits.

COs–CO3

Self Learning Topics: Need of clock signal in sequential circuits. Applications of Bistable Circuits.

UNIT-IV: MEMORY ARCHITECTURES **14 Hours**

Data path circuits, Architectures for Adders, Multipliers, Shifters, Speed and Area Tradeoffs, Array Subsystems: SRAM, DRAM, ROM. **COs–CO4**

Self Learning Topics: Comparison of PROM, EPROM, EEPROM

UNIT -V: ARCHITECTURE DESCRIPTION **14 Hours**

Introduction, Power distribution, Input/Output, Clock, Hardware Description Languages, Verilog HDL: Behavioral modeling, Structural gate modeling, Switch modeling, Basic constructs, FSM, High-level synthesis. **COs–CO5**

Self Learning Topics: Comparison between SMI, MSI, LSI, VLSI,ULVSI

Board of Studies : Electronics and Communication Engineering
Approved in BoS No. : 02, 30th May, 2025
Approved in ACM No: 02

Text Books:

1. Jan M Rabaey, Anantha Chandrakasan, B Nikolic, Digital Integrated Circuits: A Design Perspective, Second Edition, 2003, Prentice Hall of India.
2. Niel H.E. Weste, David Harris, Ayan Banerjee, CMOS VLSI Design- A circuits and Systems Perspective, Third Edition, 2013, Pearson education.

Reference Books:

1. Chris Spear, System Verilog for Verification, Springer, 2006.
2. Wayne Wolf, Modern VLSI Design, PHI Learning Private Limited, New Delhi, 2011.
3. Sung-Mo Kang and Yusuf Leblebici, CMOS Digital Integrated Circuits, McGraw Hill, 3rd Edition, 2011.

Web References:

1. https://onlinecourses.nptel.ac.in/noc21_ee09/preview
2. https://www.udemy.com/topic/vlsi/?p=2&srsltid=AfmBOopszPIWTThMFnTj0Oj0kZIy0XuhAWZDvS3MyZ5vvELxGlroq8NM

Internal Assessment Pattern

Cognitive Level	Internal Assessment # 1 (%)	Internal Assessment # 2 (%)
L1	30	--
L2	40	--
L3	30	30
L4	--	30
L5	--	40
Total (%)	**100**	**100**

Short and Long Answers Questions of Various Cognitive Levels:

L1: Remember

1. Define the static and dynamic characteristics of a MOSFET transistor.
2. What are the basic principles of dynamic CMOS design?
3. What is the difference between static and dynamic latches? Provide examples of each.
4. What are the basic types of adders used in digital circuits, and how do they differ in terms of functionality?
5. What is the role of hardware description languages (HDLs) in digital system design?

L2: Understand

1. Explain the behavior of a MOSFET under static and dynamic conditions. How do these conditions affect the performance of CMOS circuits?
2. Describe the operation of pass-transistor logic in CMOS circuits and highlight its advantages and limitations.
3. Explain the significance of timing metrics in the performance evaluation of sequential circuits.
4. Explain how a binary multiplier works and its role in arithmetic data path circuits.
5. Describe the difference between behavioral and structural modeling in Verilog HDL. Provide an example of each.

L3: Apply

1. Design a pass-transistor logic circuit to implement a 2-input AND gate and explain its operation.
2. Given a set of specifications, design a static D flip-flop using CMOS technology and calculate its setup and hold times.
3. Implement a simple pipeline architecture using static registers and evaluate its performance in terms of throughput and latency.
4. Implement a 4-bit shifter circuit using CMOS logic and evaluate its performance in terms of speed and area.
5. Write a Verilog code for a simple 4-bit counter using behavioral modeling. Explain the functionality of the code

L4: Analyzing

1. Analyze how secondary effects like channel length modulation and short-channel effects impact the performance of a CMOS inverter.
2. Analyze the advantages and disadvantages of complementary CMOS logic compared to ratioed logic in terms of power consumption and noise margins.
3. Analyze the impact of clock skew and propagation delay on the timing metrics of sequential circuits. How do these factors affect the setup and hold time of a register?
4. Compare the performance of different memory architectures (SRAM, DRAM, ROM) in terms of access time, power consumption, and area efficiency for use in embedded systems.
5. Analyze the impact of improper clock distribution on the performance of a VLSI chip. How does this affect timing and power consumption?

L5: Evaluating

1. Evaluate the performance of different combinational logic circuit design styles (e.g., complementary CMOS, ratioed logic, pass-transistor logic).

2. Compare and contrast the advantages and disadvantages of static and dynamic CMOS design.
3. Assess the impact of noise and variability on combinational logic circuit performance.
4. Evaluate the trade-offs between speed, power consumption, and area in combinational logic circuit design.

Chairperson
Board of Studies (ECE)

MTVDOE2104 **EMBEDDED SYSTEMS** **3 0 0 3**

(Open Elective-1)

Course Objectives:

- Understand the fundamentals of embedded systems, including their definition, history, classification, and application areas.
- Design and develop embedded systems using various components, such as processors, ASICs, PLDs, and memory.
- Develop embedded firmware using reset circuits, brown-out protection circuits, oscillator units, and watchdog timers.
- Apply RTOS-based embedded system design principles, including task scheduling, communication, and synchronization.
- Select and implement suitable RTOS for embedded system development, considering factors such as task communication, synchronization, and device drivers.

Course Outcomes:

At the end of the course, students will be able to:

Course Code	Course Outcomes	Mapping with POs and PSOs						
		PO1	PO2	PO3	PO4	PO5	PO6	DoK
MTVDOE2104.1	Understand pseudo NMOS logic circuits and calculate inverter threshold voltage, output high voltage, and output low voltage.	3	3	2	1	0	1	L1, L2
MTVDOE2104.2	Design and implement combinational logic circuits using NMOS and CMOS gates to realize Boolean expressions.	3	3	2	1	0	2	L3
MTVDOE2104.3	Design and analyze clocked latch and flip-flop circuits, including CMOS D latch and edge-triggered flip-flop.	3	3	3	2	0	2	L3, L4
MTVDOE2104.4	Analyze basic principles of dynamic logic circuits and design dynamic CMOS transmission gate logic circuits	2	2	2	1	0	1	L4
MTVDOE2104.5	Compare and contrast different types of semiconductor memories, including RAM and flash memory, and analyze their operation.	3	2	1	1	1	2	L4, L5

SYLLABUS

UNIT I Introduction to Embedded Systems **12 Hours**

Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics of Embedded Systems. **CO's-CO1**

Self Learning Topics: Quality Attributes of Embedded Systems.

UNIT II Typical Embedded System **16 Hours**

Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators. Communication Interface: Onboard Communication Interfaces. **CO's-CO2**

Self Learning Topics: External Communication Interfaces.

UNIT III Embedded Firmware **14 Hours**

Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages. **CO's-CO3**

Self Learning Topics: Need of Oscillator Unit

UNIT IV RTOS Based Embedded System Design **11 Hours**

Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, **CO's-CO4**

Self Learning Topics: Task Scheduling.

UNIT V Task Communication and Task Synchronization **15 Hours**

Shared Memory, Message Passing, Remote Procedure Call and Sockets. Task Communication / Synchronization Issues, Task Synchronization Techniques, Device Drivers, Methods to Choose an RTOS. **CO's-CO5**

Self Learning Topics: Advantages of Shared Memory

Board of Studies: Electronics and Communication Engineering

Approved in BOS No: 02, 30th May, 2025

Approved in ACM No: 02

Text Books:

1. "Embedded Systems" by Raj Kamal (McGraw Hill Education)
2. "Embedded Systems: Architecture, Programming, and Design" by Rajib Mall (McGraw Hill Education)
3. "Embedded Systems: Real-Time Operating System for ARM Cortex-M Microcontrollers" by Jonathan W. Valvano (Create Space Independent Publishing Platform)

Reference Books

1. "The Art of Designing Embedded Systems" by Jack Ganssle
2. "Embedded Systems: A Contemporary Approach" by James M. Lampsas
3. "Real-Time Systems: Development and Implementation" by Jiming Chen

Internal Assessment Pattern

Cognitive Level	Internal Assessment # 1 (%)	Internal Assessment # 2 (%)
L1	30	--
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L3	40	30
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L5	--	30
Total (%)	**100**	**100**

L1: Remembering

1. What is an embedded system?
2. List the characteristics of embedded systems.
3. What is the purpose of a watchdog timer?
4. Define RTOS.
5. Name different types of memory used in embedded systems.

L2: Understanding

1. Explain the difference between embedded systems and general computing systems.
2. Describe the role of sensors and actuators in embedded systems.
3. How does a reset circuit work in an embedded system?
4. What is the significance of task scheduling in RTOS?
5. Compare and contrast different types of operating systems.

L3: Applying

1. Design a simple embedded system for a specific application.
2. Choose suitable memory types for a given embedded system application.
3. Implement a task scheduling algorithm for a given RTOS.
4. Develop a simple device driver for a specific peripheral.
5. Use a specific RTOS for a given embedded system project.

L4: Analyzing

1. Analyze the trade-offs between different types of memory in embedded systems.
2. Compare the performance of different RTOS scheduling algorithms.
3. Evaluate the impact of different communication interfaces on embedded system performance.
4. Identify potential issues with task synchronization in a given RTOS-based system.
5. Analyze the stability of a given embedded system design.

L5: Evaluating

1. Evaluate the performance of a given embedded system design.
2. Compare and contrast different embedded system design approaches.
3. Justify the choice of a specific RTOS for a given application.
4. Assess the reliability and stability of a given embedded system design.
5. Evaluate the security of a given embedded system design.

Chairperson
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